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Designing of Extra Low Power Multiple Transistor with Single-Phase Clocking FF Designs with Improved Performance

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***Abstract*—In this paper the authors come up with a very modern, high-speed 18-transistor true single phase clocking D flip-flop (FF) design using complementary pass-transistor logic. This design is a master-slave logic structure and hybrid logic design that combines a consistent pass-transistor style with a CMOS standalone style. In order to reduce the number of transistors and to simplify the complexity of the circuit using a corresponding pass-transistor style. In this design environment the conversion is faster on the slave latch which improves time performance using the visual VDD method. The cycle is designed using GPDK 60nm CMOS technology and the simulation results show better performance indicators such as moderate power consumption, clock delay to Q, data delay to Q, PDP and operating environment. In any digital circuit design, one of the most common and important building blocks is Flip Flops. Energy, performance, space are factors that affect design. An effective design should be developed by three parameters. The design of the time frame focuses on improving strength and performance. The features of the PPA (Power Workplace) can be enhanced with many techniques. In this low power sheet 18-Transistor single phase FF design clock is recommended. Master-Slave configuration is used to design FF. It is built using flexible CMOS and complementary pass transistors logic. FF is designed to reduce the use of flexible energy by avoiding floating internal nodes. The microwind and DSCH software is used for Flip Flop implementation with 1V VDD voltage and 500MHz clock frequency. FF design uses 50nm technology. The effects of power dissipation and delay compared to 19-TSPC The results of the proposed project were found to be more efficient than other FF projects by comparison. Compared with the TSPC, the PDP development of the proposed project was 68% and 73% of the total dynamic clock, respectively, with a low leakage of 27%.**

***Keywords*— Adaptive active damper, grid connected inverters, harmonic current reference compensation technique, PI controller, DSMPI Controller.**

I. INTRODUCTION

In the development of high-level integration (VLSI), the latest updates on powerful battery-powered mobile devices such as personal digital assistants (PDAs) and mobile phones set new targets. These principles include the need for high-speed digital circuits using low power. In any clock system flip-flops and latches of time elements are responsible for using less power & advanced latency over building blocks, they become the most important components in a compatible VLSI system. A flip-flop or latch is an electronic circuit that can be used to store digital information - a multivibrator ebitable. A cycle can be created to change the situation by using signals in one or more control inputs and receiving one or two outputs. Flip-flops are a basic unit for making digital models. Each flip flop involves a single bit of storage, which are integrated model processes and the functionality of a given clock frequency will be synchronized. Flip flop is either an activated edge point or a negative edge activated which indicates that the input has an output when the clock starts from the top log to the bottom or bottom up, respectively. Flip flops are of two types on the basis of data storage. Flip flops mounted on a single edge can be defined as a flip - a flop that holds data on the straight edge or the negative edge of the clock signal. Flip-flops are two-dimensional flip-flops that store data on both the positive and negative edge of the clock signal. The flip-flop has two circuits where one circuit represents "one" and the other represents "zero". Flip-flop used in finite-state machine, where the next & output status depends not only on your current input, but also on your current status. Flip-Flop can also be used to calculate pulses and to adjust dynamic input timers. Digital designs typically use deep piping techniques and offer many FF-rich modules such as first out (FIFO), shift register, and registry file and shift register. It is also surprising that the power consumption of the clock system is as high as 50% of the total system power that is compatible with clock

distribution networks and storage devices. FFs therefore allow for a large proportion of chip space and energy consumption in the entire system configuration. Various techniques and several flip-flops have recently been introduced to reduce duplication in the system / clock system. There are various flip-flops provided in the books. Several digital and computer circuits using pulsed-triggered flip-flops can be one or two and the main slave.

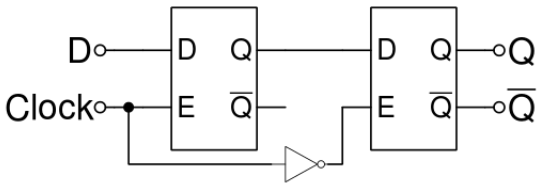

Fig 1: Master–slave edge-triggered D flip-flop block diagram

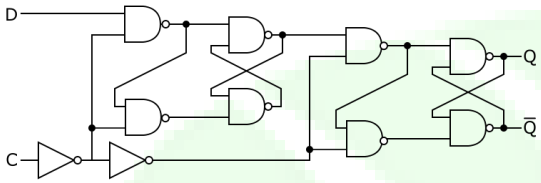

Fig 2: Master–slave edge-triggered D flip-flop

In the positive-edge activated master – slave D flip-flop, where there is a low signal clock (sensible 0) we first see the "open" or "master" D latch (distorted clock signal) high (sensible 1. if the clock signal is shifted from low up and allow the "master" latch to save the input value. As the clock signal rises from 0 to 1 "allow" the distortion of the first latch descending from 1 to 0 and inputs. Latch value key "lock" at about the same time, "allow" the twisted latch of the second clock or "slave" from the bottom (0) to the top (1) of the clock signal. has passed the "slave". the visible value is held while the latch "master" begins to receive new values to prepare the next edge of the clock. Pulse-triggered flip-flops are used by microprocessors a few modern. The traditional master-slave flip-flops are made up of two sections, one master and one slave and the Flip-flops of the Slave comprise two classes, one master and one slave and are represented by their firmness. property. There are several examples of master-slave flip-flop that include a POWERPC 603 transmission gate, push-pull D-type-flip-flop (DFF), and a real single phase clocked (TSPC) flip-flop. Another flip-flop activated edge is a sensor amplifier based flip-flop (SAFF)

II. LITERATURE REVIEW

J. Lin et al., [1] The lowest flip-flop (FF) clock design achieved using only 19 transistors. The design follows the logical design of the master-slave-type and incorporates a rational design that incorporates both static-CMOS sensitivity and pass-transistor logic compatibility. In construction, a sensible structural reduction reduction scheme is used to reduce the number of transistors in order to obtain high power and operational delays. Despite the simplicity of the circuit, no internal nodes remain floating during operation to avoid power leaks. In this design, the visual VDD design method, which enables rapid transformation of the shape in the slave latch, is designed to improve the performance over time. In circuit applications, transistor sizes are developed in relation to a powerdelay (PDP) product. The TSMC 90-nm CMOS process is selected as the operating technology. In this work, the performance standards of the seven FF projects are compared. The time limits for each FF are specified first. Post-structural simulation results have shown that the proposed design is very effective in various performance indices such as PDP, clock delay to Q, medium power consumption, and leak power consumption. In addition, the design was limited to a small planning space. Compared with the standard FF project based on the transfer gate, the development of the PDP in the proposed project was 63.5% (12.5% shift work) and spatial savings of almost 10%. Additional simulations in process corners, supply power settings, and operating waves were performed to study design reliability.

W. Wang et al., [2] It is proposed to double the voltage distribution of the low voltage based on the expansion of the base of the single-phase real clock (E-TSPC). By reducing the number of consecutive transistors from VDD to GND, the proposed structures can operate effectively at low voltage. The simulation results in the new SMIC 40nm show that the structure shown has better power and faster use with lower power supply. Compared to the identified frames, the introduced system II can operate at very low supply voltage with minimal operating loss.

J. Shaikh et al., [3] Positron emanation tomography (PET) is an effective atomic imaging technique that delivers a three-dimensional image of the organs used in the body. PET requires high goals, an analog of high speed and low power to digital converter (ADC). The multichannel ADC running of the PET scanner grinding machine covers several squares. Most squares can be organized using fast, low D-flip flops. One pre-set phase clock (TSPC) D flip-flop shows various errors (disturbances) in production due to unintentional fluctuations between road hubs. Preset-capable modified TSPC (MTSPC) D flip-flop has been suggested as the preferred solution to reduce this problem. However, the MTSPC D flip-flop requires one additional PMOS to stop switching between road hubs. For this task, we set up a pre-set 7-bit coded code calculator using the proposed D flip-flop. This function includes a new UMC 180 nm CMOS processor for a 7-bit black code that can be pre-configured where we achieve maximum 1 GHz duplicate function with a maximum throughput (MSB) of 0.96 ns, a power consumption of 244.2 μW (watt scale) and power dissipation (PDP) 0.23 pJ (Pico joule) from 1.8 V.

P. Xu et al., [4] True Single Phase Clock (TSPC) flip-flops (FF) are commonly used in repetitive dividers due

to their high performance speed and low power compared to the owner Ace Slave FFs. In this work, we study the continuous development of TSPC repeater separators in the division of slow clocks into Ultra-low-power (ULP) SoCs. We break down engineering, career guidance and the problem of unfortunate knowledge in a repetitive TSTV-based separator. A development approach based on increasing the length of a particular gate is proposed to limit energy consumption by adjusting the exchange and energy consumption. A 10-fold repeater separator was set to 28 nm FDSOI CMOS and integrated into the ULP SoC. Rear format formatting and 32-MHz input duplicate shows power consumption of 28.3 nW and supply voltage of 0.8-V.

F. Stas et al., [5] In this work, we propose an 18-transistor (18T) True-Single-Phase-Clock (TSPC) Flip-Flop (FF) with fixed data retention based on two forward-facing criticisms. circles, without increasing the load on the clock, in contrast to the standalone design of the TSPC. The proposed FF was used for ultra-low-voltage (ULV) operation at 28nm FDSOI CMOS. Proposed FF displays separated by clock separation scales are compared with reference structures including standard M-S FF, standard TSPC FF and the final proposed TSPC FF. Compared to conventional MS FF, the proposed FF separately displays 5%, 60% and 30% enhancements at 0.4V with maximum frequency, power / cycle and dissipation power.

J. Lin et al., [6] In this work, a proposed single-phase low-power flip-flop (FF) clock is proposed using only 19 transistors. This system follows the design concept of the ace type slave and highlights a partial and partial rational configuration that includes both static-CMOS rationale and integral pass-transistor rationale. In this system, a logical reduction reduction system is used to reduce the number of transistors in order to achieve maximum power and to delay performance. Despite its circuit accuracy, no internal harbors are left along the shore during operation to avoid waste energy use. In this structure, a visual VDD system approach, which promotes rapid state progress in slave locking, is conceived to enhance the execution of time. In circuit applications, transistor sizes are arranged in relation to a powerdelay (PDP) object. TSMC 90-nm CMOS process

III. PROBLEM FORMULATION

3.1 DIGITAL CIRCUITS

Many integrated circuits (ICs) that do not meet satisfactory standards use the clock signal for the real purpose of synchronizing various pieces of the circuit, cycling at a slower rate than the worst of the stimulus delays. Sometimes, more than one clock rotation is required to play a previewed motion. As ICs end up being more impressive, the issue of providing careful and harmonious clocks across all circuits is becoming increasingly confusing. A rare phenomenon of such complex chips is a microchip, the central component of modern PCs, which relies on a clock from an important stone oscillator. Unusual system unusual situations for non-simultaneous circuits, for example, over-CPUs.

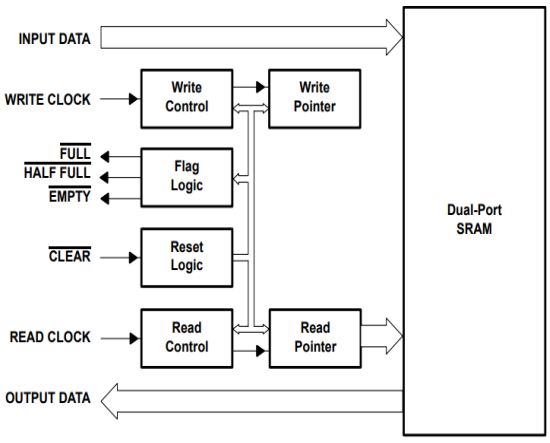

Figure 3.1 Block diagram of FIFO with storage

In Figure 3.1, the long fall in long FIFOs, the design should not re-transmit data names to all memory locations. The issue is understood by indirect memory with two pointers. In FIFO's indirect thinking, the memory address of the data is still a creative identifier. The location of the main data name in the FIFO to be tested is in the location of the indexed object. After the reset, the two indicators show the same memory location. After performing each task, a point point is set to the next memory location. Data name test sets the read identifier into the next data name to be processed. The read index does not always require a creative index. Once the readable pointer goes to the make pointer, FIFO is empty. When the form indicator rises sharply with the read index, FIFO is full.

3.1.1 One-phase clock

Most compatible current circuits use only "single phase clock" - at the end of the day, they transfer the entire clock flag (successfully) by 1 call.

3.1.2 Two-phase clock

In synchronous circuits, a "two-phase clock" implies clock sign dispersed on 2 wires, each with non-covering pulses. Customarily one wire is assigned "phase 1" or "φ1", the other wire passes on the "phase 2" or "φ2" signal. Since the two phases are guaranteed non-covering, gated bolts instead of edge-actuated flip-flops can be used to store state information to the extent that the commitments to snares on one phase simply depend upon yields from locks on the other phase. Since a gated lock uses only four entryways versus six portals for an edge-actuated flip-flop, a two phase clock can prompt an arrangement with a more diminutive as a rule entryway count anyway when in doubt at some discipline in a tough situation and execution.

3.1.3 4-phase clock

A "4-phase clock" has clock sign dispersed on 4 wires (four-phase justification). In some early chip, for instance, the National Semiconductor Demon 16 family, a multi-phase clock was used. By virtue of the Pixie 16, the clock had four phases, each 90 degrees isolated, with

the ultimate objective to synchronize the errands of the processor focus and its peripherals.

III.PROPOSED WORK METHODOLOGY

The main contribution of the proposed work is as follows-

•To design ultra-Low Power 18-Transistor Single-Phase Clocked Flip-Flop in CMOS using 50nm Technology.

•To design Transmission gate FF (TGFF), static single-phase contention-free FF (S2CFF) and True Single Phase Clocking (TSPC) based on new topology.

•To analysis of designs and achieve better performance of in terms of power, area and delay

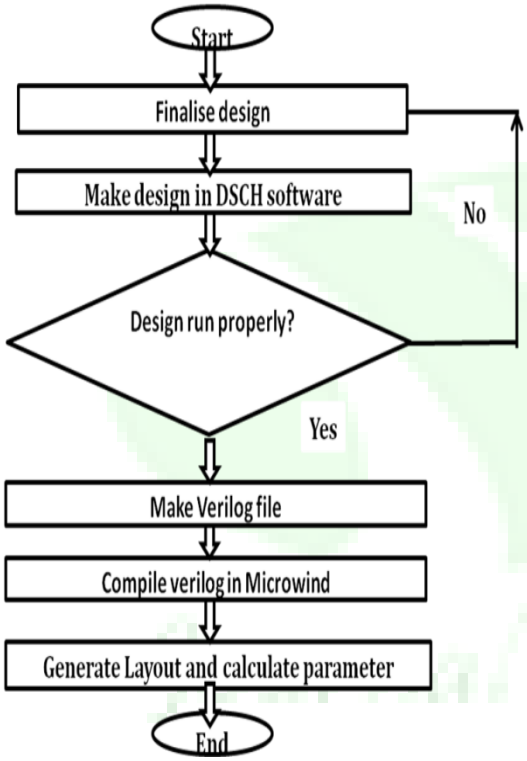

Figure 4.1: Flow Chart

4.1.1 ALGORITHM

Step 1- Firstly make design in DSCH software using available component then make connection between them as per requirement.

Step 2- Now press run simulation and see output in terms of LED glow or not, if input and clock is on and led glow then designed circuit give proper output otherwise there are some errors in circuit.

Step 3- Now save this design and make verilog file, then a verilog file will be generated automatic.

Step 4- Open Microwind software and compile verilog file. Then generate CMOS layout. Now calculate parameters and compare result.

4.2 METHODOLOGY

This work proposes 18-transistor SPC (18TSPC), a SPC FF with only 18 transistors (the lowest reported for a fully static contention-free SPC FF) with a novel master-slave Fig. 3. Simulation results show TCFF internal node voltages at (a) VDD = 1.2 V and (b) VDD = 0.6 V when D rising at CK = 0 [15]. topology With a simplified topology, it delivers a 20% reduction in cell area compared to TGFF. Unlike SoA designs, 18TSPC meets all ultra-low power FF design requirements. It has been implemented in 65-nm CMOS along with a TGFF. This proves EDA compatibility and demonstrates circuit and system-level benefits. The design was first simulated then experimentally validated at 0.7 V, 25 ◦C, at various data activity rate (α), showing that the proposed 18TSPC achieves reductions of 68% and 73% in overall (Pα=10%) and clock dynamic power (Pα=0%), respectively, and 27% lower leakage compared to TGFF. Furthermore, unlike TCFF, the measurements indicate superior 18TSPC in performance.

SPC FF Design Approach The aim of the design is to carry forward the enhancements achieved by previously reported FFs in terms of cell area, power consumption, and performance but to overcome the limitations of these designs. To do this, the initial step is to evaluate the Boolean function of a positive-edge trigged master-slave FF (MSFF) Dpresent ML = CK • D + CK • Dprevious ML (1) Dpresent SL = CK • Dprevious SL + CK • Dpresent ML (2) In (1), D is the data input, Dpresent ML is the present data in the master latch, and Dprevious ML is the data which has been latched from D during the previous low CK. In (2), Dpresent SL is the present data in the slave latch and Dprevious SL is the data which has been latched from the output of the master latch during the previous high CK in the slave latch.

4.2.1 Clock Generation for System-On-Chip

System- Framework on-chip advanced to all the while meet "More Moore" and "More than Moore" needs of the buyers. A Framework on-chip (SoC) is an IC structured by sewing together various remain solitary VLSI plans to give full usefulness to an application. These IP centers are pre-structured and pre-checked and made secluded to empower re-ease of use. A few centers are planned inside and some sourced from outsiders.

The centers are accessible in the accompanying sort's delicate centers –

• Reusable centers as a synthesizable RTL portrayal or a netlist of conventional library components.

• Firm centers - reusable centers that have been basically and topologically improved for execution and territory through floor-arranging and situation, maybe utilizing a scope of process innovations. These exist as integrated code or as a netlist of conventional library components.

• Hard centers - reusable centers that have been streamlined for execution, power and size, and mapped to a particular procedure innovation.

The term 'clock age' utilized conversely with the term 'recurrence combination's alludes to the technique by which the clock required for a specific IP center is created from a reference clock (more often than not a precious stone oscillator). They might be delegated

IV.SIMULATION RESULT &ANALYSIS

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The implementation and simulation of the proposed designs is done over DSCH-Microwind software. The DSCH software has various menus and help bar, where different gates, supply, ground etc are available. Microwind software also has the function which converts DSCH design into verilog files and layout diagram.

5.1 SIMULATION SOFTWARE

The DSCH program is a rationale editorial manager and test system. DSCH is utilized to approve the engineering of the rationale circuit before the microelectronics configuration is begun. DSCH gives an easy to use condition to various leveled rationale plan, and quick recreation with defer investigation, which permits the structure and approval of complex rationale structures.

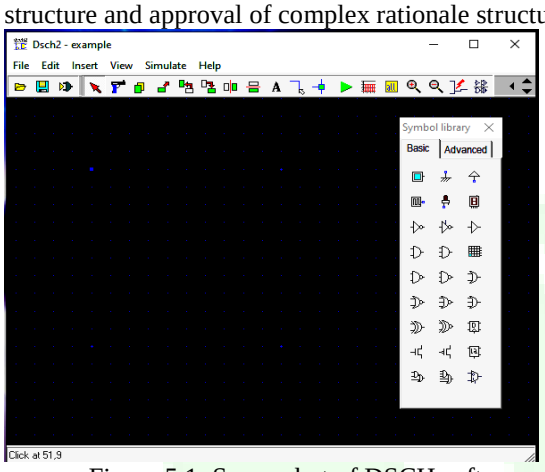


Figure 5.1: Screenshot of DSCH software

DSCH likewise includes the images, models and get together help for 8051 and PIC16F84 controllers. Planners can make rationale circuits for interfacing with these controllers and confirm programming programs utilizing DSCH.

MICROWIND is really coordinated EDA programming enveloping IC plans from idea to finishing, empowering chip originators to structure past their creative mind. MICROWIND coordinates generally isolated front-end and back-end chip structure into one stream, quickening the plan cycle and decreases plan complexities.

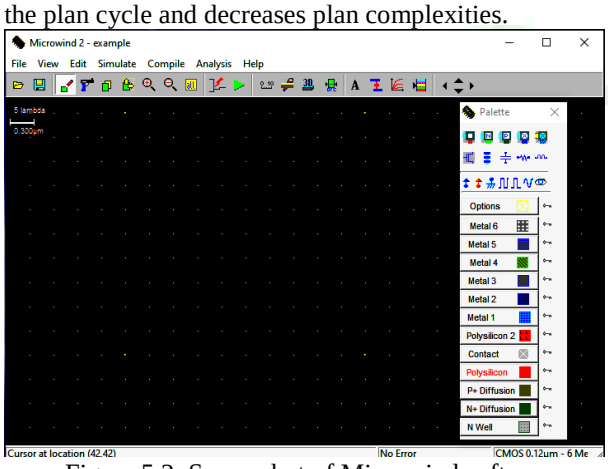


Figure 5.2: Screenshot of Microwind software

It firmly coordinates blended sign usage in with computerized execution, circuit recreation, transistor-level extraction and confirmation – giving creative training activity to assist people with developing the aptitudes required for configuration positions in for all intents and purposes each space of IC industry. FinFET has been presented in Microwind new 3.8 rendition, with Format, size and exhibitions roused from 14-nm FinFET innovation.

5.2 PROPOSED DESIGNS

5.2.1 Conventional Transmission Gate FF

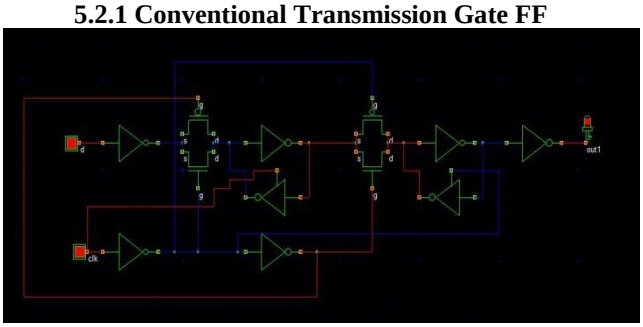


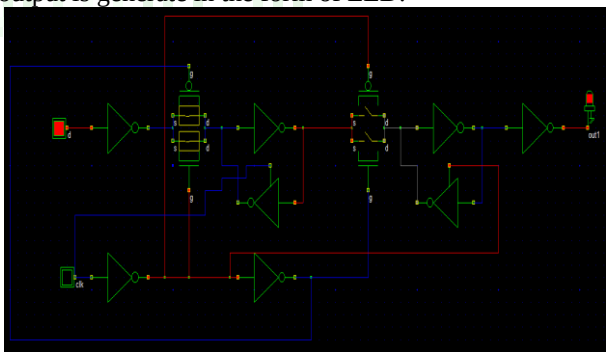
Figure 5.3: Design of TGFF and output-1

Figure 5.3 showing design of conventional transmission gate FF. AND gate, PMOS and CMOS component are using to design this circuit. To check result, when clk=1 d=1 then output=1. This circuit is used the D flip flop. The simulation scenario is proved by the truth table of D flip flop.

Table 5.1: Truth table of D flips flop TGFF

Clk	D	Q	$\bar{Q}$
0	0	Q	$\bar{Q}$
0	1	Q	$\bar{Q}$
1	0	0	1
1	1	1	0

So in this case as we apply the high state in D and clock pulse then the output is also high. If the clock signal is low then output is also low. When the input of D is high and clock is low then the output is also high. On the other hand whatever signal state is applied in D, as same output is generate in the form of LED.



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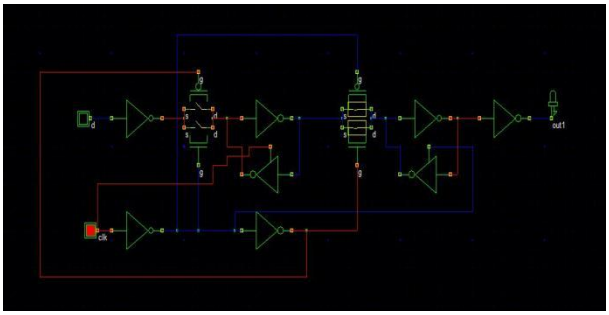

Figure 5.4: Design of TGFF and output -2

when clk=1 d=0 then output=0 and clk=0 d=1 then output=1. So its satisfied the truth table of D flip flop. Therefore this is satisfied the truth table of D flips flop.

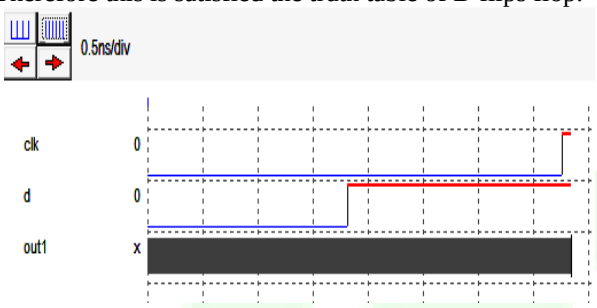

Figure 5.5: Timing diagram of TGFF design

Timing Diagram for a D Type Master-Slave Flip-flop. Considering the master slave flip-flop as a single device, the relationship between the clock (CK) input and the Q output does look rather like a negative edge triggered device, as any change in the output occurs at the falling edge of the clock pulse.

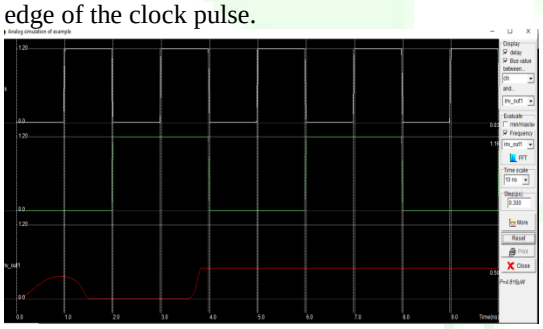

Figure 5.6: Voltage vs time plot

Figure 5.5 and figure 5.6 are showing timing and output graph. Therefore it can be seen that when apply input and clock then output will be enable.

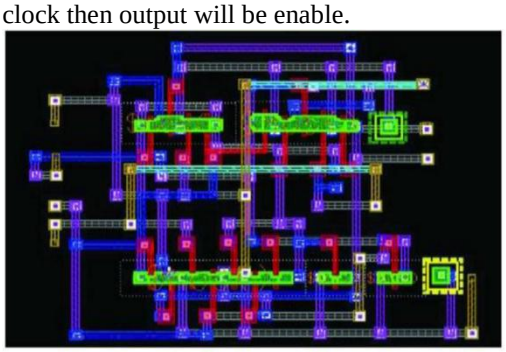

Figure 5.7: Layout of TGFF

Figure 5.7 presentation CMOS layout design of TGFF, it includes various metal, PMOS, NMOS and contact points.

Table 5.2: Simulation Parameter of TGFF

Sr No.	Parameters	Value
1	Area	222.7µm2
2	Power	4.816 µW
3	Delay	5ns
4	Power Delay Product (PDP)	240.8
5	Rise time	0.025ns
6	Fall time	0.025

5.2.2 Single phase contention free FF (S2CFF)

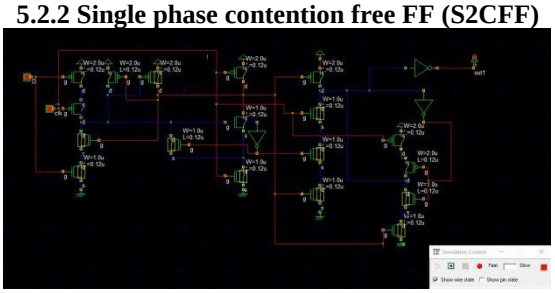

Figure 5.8: Design of static single-phase contention-free FF (S2CFF) and output-1

Figure 5.8 showing design of static single-phase contention-free FF. AND gate, PMOS and CMOS component are using to design this circuit. To check result, when clk=1 d=1 then output=1.

Table 5.3: Truth table of D flips flop S2CFF

Clk	D	Q	$\bar{Q}$
0	0	Q	$\bar{Q}$
0	1	Q	$\bar{Q}$
1	0	0	1
1	1	1	0

So in this case again we apply the high state in D and clock pulse then the output is also high. If the clock signal is low then output is also low. When the input of D is high and clock is low then the output is also high. On the other hand whatever signal state is applied in D, as same output is generate in the form of LED.

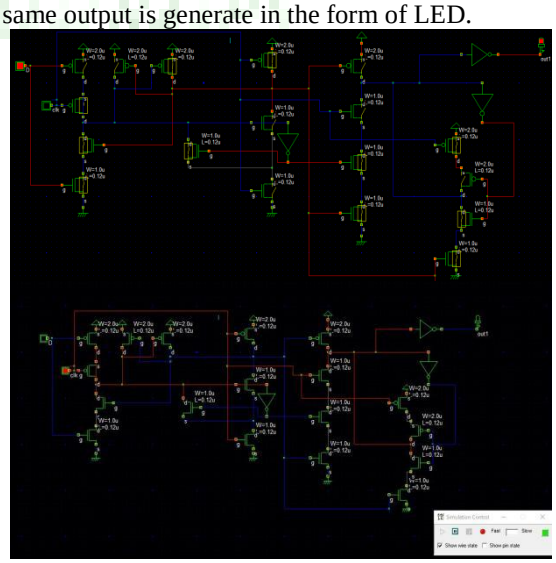

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Figure 5.9: Design of S2CFF and output-2

When clk=1 d=0 and output=0, another condition when clk=0 d=1 and output=1

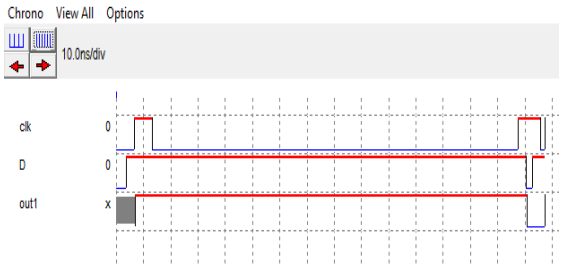

Figure 5.10: Timing Diagram

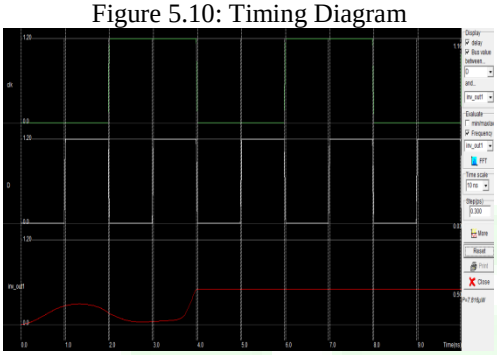

Figure 5.11: Voltage vs time graph of S2CFF

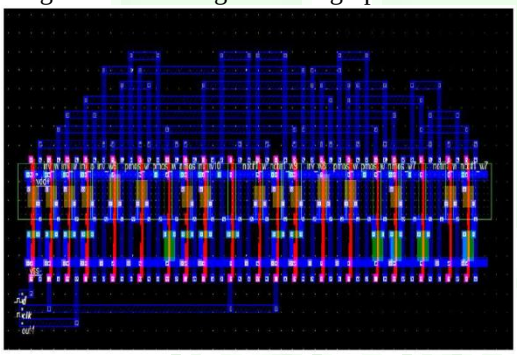

Figure 5.12: Layout of S2CFF

Sr No.	Parameters	Value
1	Area	427.2µm2
2	Power	7.816µW
3	Delay	8ns
4	Power Delay Product (PDP)	625.28
5	Rise time	0.025ns
6	Fall time	0.025ns

5.2.3 18-transistor single-phase clocked (TSPCFF)

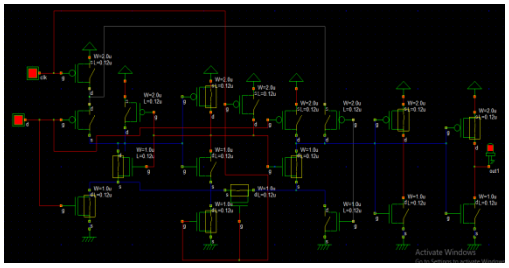

Figure 5.13: Proposed 18-transistor single-phase clocked (TSPCFF) and output-1

Figure 5.13 showing design of transistor single-phase clocked. AND gate, PMOS and CMOS component are using to design this circuit. To check result, when clk=1 d=1 then output=1.

Table 5.5: Truth table of D flips flop TSPCFF

Clk	D	Q	$\bar{Q}$
0	0	Q	$\bar{Q}$
0	1	Q	$\bar{Q}$
1	0	0	1

So in this case as again apply the high state in D and clock pulse then the output is also high. If the clock signal is low then output is also low. When the input of D is high and clock is low then the output is also high. On the other hand whatever signal state is applied in D, as same output is generate in the form of LED.

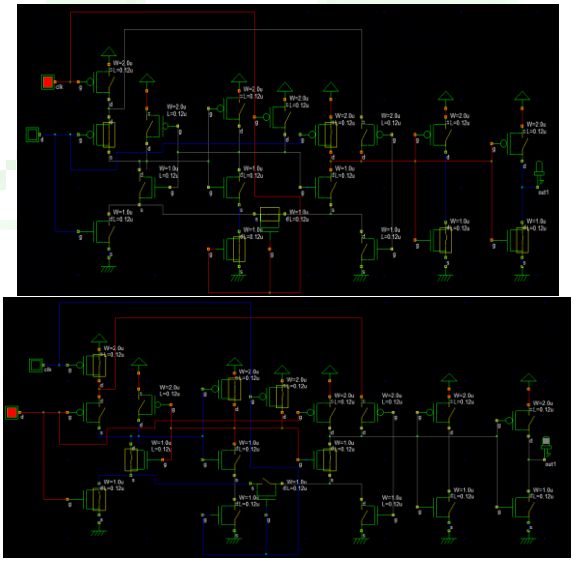

Figure 5.14: Proposed 18-TSPCFF and output-2

Figure 5.14 presenting, 18-TSPCFF when clk=1 d=0 and out=0, and when clk=0, d=1 then output=1.

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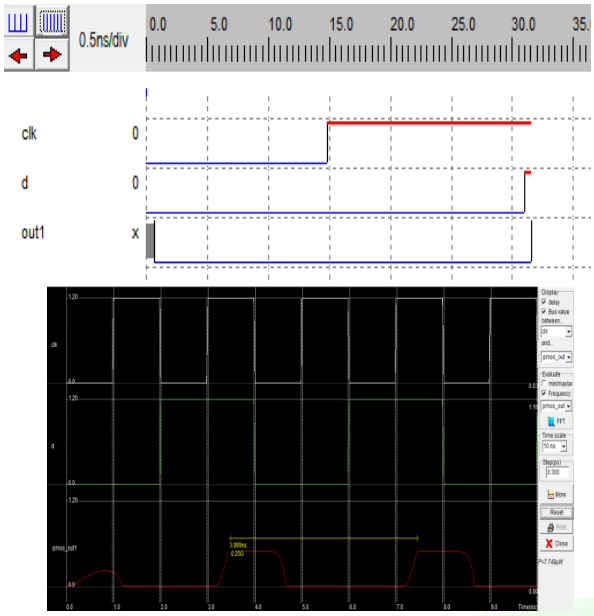

Figure 5.16: Voltage vs time of 18-TSPCFF

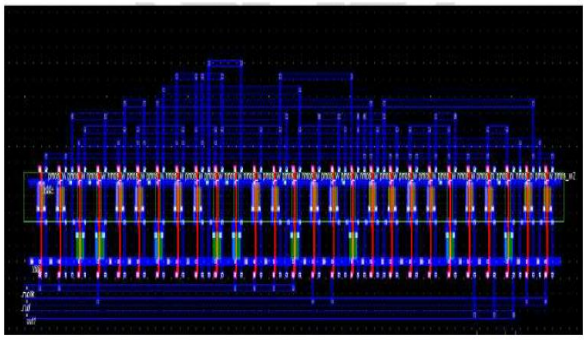

Figure 5.17: Layout of 18-TSPCFF

S.N	Parameters	Value
1	Area	374.0µm
2	Power	7.749µW
3	Delay	7ns
4	Power Delay Product (PDP)	542.43
5	Rise time	0.025ns
6	Fall time	0.025ns

Table 5.6: Simulation Parameter of 18-TSPCFF

Table 5.7: Comparison of proposed designs result with previous designs

S.N	Parameter	Existing Designs			Proposed Design		
1	Design	TGFF	S2CFF	19-TSPC	TGFF	S2CFF	18-TSPC
2	Technology	90 nm	90 nm	90 nm	50 nm	50 nm	50 nm
3	Topology	Gate level	Gate level	Gate level	Compressed Topology	Compressed Topology	Compressed Topology
4	Area (um^2)	3331	3388	3265	222.7	427.2	374
5	Power(uW)	65	70	30	4.21	6.30	6.54
6	Delay (ns)	10.73	20.73	13.28	5	8	7
7	Setup Time(ns)	4.66	14.7	9.2	0.25	0.25	0.25
8	Hold Time(ns)	2.9	10.2	11	0.25	0.25	0.25

Figure 5.18: Delay plot of previous vs proposed design

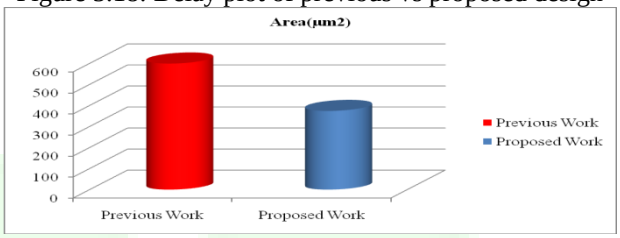

Figure 5.19: Area plot of previous vs proposed design

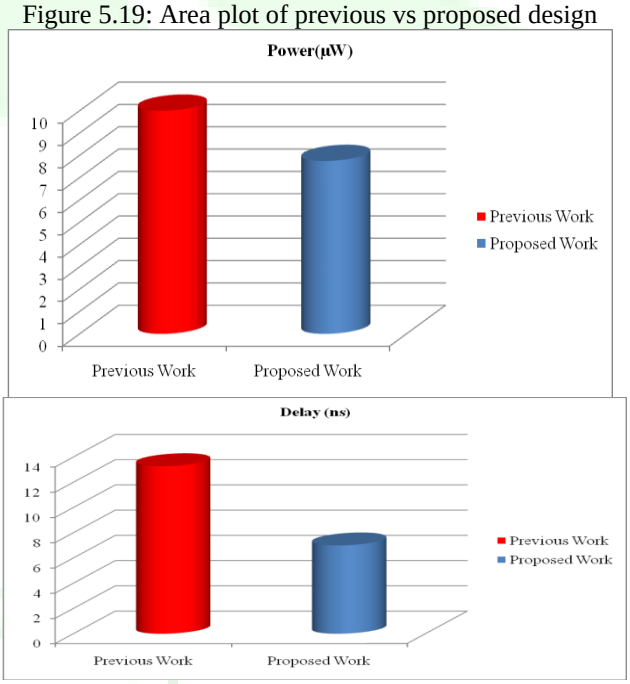

Figure 5.20: Power plot of previous vs proposed design

Therefore to see all simulated result and parameter values, it is observed that proposed design performance is better than previous designs

V.CONCLUSION AND FUTURE WORK

Set-up time, capture time, clock-to-output delay time (clock-Q delay to time), and power consumption of TSPC flip flops are compared and analyzed. Setup time and clock delay on the outflow of two flipflops are the same. The catch time of the proposed flip-flop in the common corner (TT) has increased by 9ps compared to those of the standard TSPC flip-flop. Total power consumption decreased by 8.3% flip-flop compared to that of conventional TSPC.

This study proposed 18TSPC, a completely stable and uncomplicated SPC FF with a reported low number of transistors (18), indicating a reduction in cell space relative to normal TGFF. Although operational penalty is observed, due to the low power factor of the proposed design, 18TSPC gains more. A brief summary of the proposed 18TSPC and a comparison of previous activities is presented. The proposed 18TSPC therefore has better power features than ever before.

The design of this research work is TGFF, S2CFF and 18-TSPC using 50 nm technology. Proposed designs use compressed topology. The operating area is 222.7, 427.2 and 374 mm2. The power consumption of the projects is 4.21, 6.30 and 6.54 W. Project delays are 5, 8 and 7 nS. Setup and hold time is 0.25nS.

FUTURE WORK

- We can make more designs using TSPC based on other research papers.
- TSPC performance can be more improved using some novel techniques.
- Various Software technologies can be used like 20nm, 30nm, 90nm etc for design performance checking.
- FPGA implementation can be done in testing lab.

REFERENCE

[1]. J. Lin, M. Sheu, Y. Hwang, C. Wong and M. Tsai, "Low-Power 19-Transistor True Single-Phase Clocking Flip-Flop Design Based on Logic Structure Reduction Schemes," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 11, pp. 3033-3044, Nov. 2017.

[2]. W. Wang, S. Jia, Z. Wang, T. Pan and Y. Wang, "Low Voltage Dual-Modulus Frequency Divider Based on Extended True Single-Phase Clock Logic," *2018 IEEE International Conference on Electron Devices and Solid State Circuits (EDSSC)*, Shenzhen, 2017, pp. 1-2.

[3]. J. Shaikh and H. Rahaman, "High speed and low power preset-able modified TSPC D flip-flop design and performance comparison with TSPC D flip-flop," *2018 International Symposium on Devices, Circuits and Systems (ISDCS)*, Howrah, 2018, pp. 1-4.

[4]. P. Xu, C. Gimeno and D. Bol, "Optimizing TSPC frequency dividers for always-on low-frequency applications in 28nm FDSOI CMOS," *2017 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, Burlingame, CA, 2017, pp. 1-2.

[5]. F. Stas and D. Bol, "A 0.4V 0.08fJ/cycle retentive True-Single-Phase-Clock 18T Flip-Flop in 28nm FDSOI CMOS," *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, MD, 2017, pp. 1-4.

[6]. J. Lin, M. Sheu, Y. Hwang, C. Wong and M. Tsai, "Low-Power 19-Transistor True Single-Phase Clocking Flip-Flop Design Based on Logic Structure Reduction Schemes," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 11, pp. 3033-3044, Nov. 2017.

[7]. H. Ashwini, S. Rohith and K. A. Sunitha, "Implementation of high speed and low power 5T-TSPC D flip-flop and its application," *2016 International Conference on Communication and Signal Processing (ICCSP)*, Melmaruvathur, 2016, pp. 0275-0279.

[8]. S. Jia, Z. Wang, Z. Li and Y. Wang, "A novel low-power and high-speed dual-modulus prescaler based on extended true single-phase clock logic," *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, Montreal, QC, 2016, pp. 2751-2754.

[9]. S. S. Varma, A. Sharma and B. Anand, "An efficient methodology to characterize the TSPC flip flop setup time for static timing analysis," *2016 13th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD)*, Lisbon, 2016, pp. 1-4.

[10]. S. Jia, S. Yan, Y. Wang and G. Zhang, "Design of low-power high-speed divide-by-2/3 prescalers with improved true single-phase clock scheme," *2014 Asia-Pacific Microwave Conference*, Sendai, Japan, 2014, pp. 241-243.

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