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ISSN(ONLINE):2278 - 3814

Volume-12, Issue-12, December 2023

JOURNAL OF COMPUTING TECHNOLOGIES (JCT)

International Journal

Page Number: 01-07

Layout Design For Power Minimization In CMOS Based Full Adder Circuit In Deep Sub Micron Technology

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Abstract*—The design of two novel 1-bit 13T full adder cells along with three existing adder cells are incorporate in this paper and their complete comparison and verification has been done in terms of power dissipation, delay and power delay product (PDP) at different operating frequencies by using HSPICE tool. It is found that the existing Gate Diffusion Input (GDI) full adder provides poor performance when compared with proposed adder cell and also its equivalent layout has been generated to calculate the area of existing and proposed adder cell by using Microwind 3.5 tool. From the simulation result it is observed that the first proposed adder circuit using XOR module has achieved maximum saving of PDP 46.71% & 96.61% when compared to existing GDI adder cells respectively. The second proposed circuit using XOR and XNOR module has achieved maximum saving of PDP 74.59% & 98.38% . This article presents a comparison of high-speed and low-voltage full-adder circuits. Our approach is to build a hybrid full-adder circuit in a single unit. This article also discusses the high-speed conventional all-in-one design that combines most of MOSCAP's functions in a single unit for driving all-electric devices. He also introduced a low-power, mostly functional 1-bit full adder that uses MOS capacitors (MOSCAP) in its architecture. This technology helps reduce power consumption, propagation delay, and digital circuit area while simplifying logic design. Simulation results show that the electronic design is superior to traditional CMOS, TG and hybrid collector circuits in terms of power consumption, delay, performance power delay (PDP) and power delay (EDP). The results after the simulation setup show the superiority of the newly designed general adder circuits over the reported conventional adder circuits. The design was implemented in Cadence Virtuoso Schematic Composer on a UMC 0.18 m process model at 1.8V single-ended supply voltage and simulated on Microwind.

***Keywords*—Adder, Pass transistor, Low Power consumption, High Performance, Hybrid Logic, Transient analysis.**

I. INTRODUCTION

Images Full adder circuits turns out to be the most major circuit utilized in numerous unpredictable arithmetic operations, for example, subtraction, division, increase, exponentiation and so forth the power utilization of these squares can be decreased by lessening the power utilization of the elemental adder and the diminishment in the power utilization of arithmetic and logical unit drives decrease in power utilization of the general framework The reason for this work is to present low power adder cells which are the key parts of different math circuits. A general decrease in Power Delay Product (PDP) has additionally been gotten through this work..

A. Need of Low Power Designs in DSM

At the framework level, as synchronous execution of microchips, adder cells are the essential module in an assortment of number arithmetic units, for example, Arithmetic Logical Units (ALUs), Ripple Carry Adders (RCAs), multipliers and so forth and these viper cells lie in the basic way. As the general execution of synchronous framework relies on basic way, a considerable measure of work has been done devoted to the change of these essential modules and number arithmetic structures. Adder exhibitions can be essentially enhanced by effective usage of convey spread chain. This should be possible by enhancing structure of 1-bit full viper cell which is the

fundamental building piece of adders like convey select or convey skip adders (CSAs) and also that of swell convey adders (RCAs). Additionally better exhibitions have been gotten by utilizing enhanced quick viper structures like as convey look forward adders and restrictive total adders.
An expansive number of full adders have been outlined by scholarly and research foundations. The generally assessed execution parameters are speed, control dispersal and range. However with the development of versatile and inserted applications, control utilization has been given the primary need concerning circuit and framework execution assessments. Besides, the speed change and lessening of transistor tally has been the point of numerous adder plans. The speed of a full adder circuit dominatingly relies on the length of the basic way in a viper circuit. Longer the basic way, bigger is the convey engendering delay. Fig. 1.1 demonstrates the basic way for convey in multi-bit full adder circuit.

B. Low Power Design Requirement
Power Considerations: According to the formula:

$$Pdyn=Vdd2.fclk.\alpha nn.cn+Vdd.$$

iscn the dynamic power dissipation of a digital CMOS circuit depends on the supply voltage Vdd , the clock frequency fclk , the node switching activities αn , the node capacitances cn, the node short-circuit currents iscn , and the number of nodes n. A reduction of each of these parameters results in a reduction of dissipated power. However, clock frequency reduction is only feasible at the architecture level, whereas at the circuit level frequency fclk is usually regarded as constant in order to fulfill some given throughput requirement. All the other parameters are influenced to some degree by the logic style applied. Thus, some general logic style requirements for low-power circuit implementation can be stated at this point.

II. LITERATURE REVIEW

B. Annapoorani et al, 2022,The adders are the vital arithmetic operation for any arithmetic operations like multiplication, subtraction, and division. Binary number additions are performed by the digital circuit known as the adder. In VLSI (Very Large Scale Integration), the full adder is a basic component as it plays a major role in designing the integrated circuits applications. To minimize the power, various adder designs are implemented and each implemented designs undergo defined drawbacks. The designed adder requires high power when the driving capability is perfect and requires low power when the delay occurred is more. To overcome such issues and to obtain better performance, a novel parallel adder is proposed. The design of adder is initiated with 1 bit and has been extended up to 32 bits so as verify its scalability. This proposed novel parallel adder is attained from the carry look-ahead adder. The merits of this suggested adder are better speed, power consumption and delay, and the capability in driving. ***A. Morgenshteinet. et. al., 2002*** [1] In this paper author presented a novel technique for improvement of all the parameters which are associated with the circuit like lower power consumption this can be achieved by reducing the transistor count of the circuit therefore author has introduce a technique known as Gate Diffusion Input (GDI). The GDI technique has a huge potential to replace a conventional 28T adder circuit design in terms of area and power consumption of the circuit but circuit suffers from voltage degradation problem. This problem can be eliminated by using hybrid GDI technique.
In Hybrid GDI technique, to improve output voltage level, an additional nMOS transistor can be added with basic GDI cell as shown in Figure 3.7. The nMOS transistor is added because it passes strong „0" value. The pair of additional nMOS with pMOS of GDI cell makes a single TG cell. An inverter is used activate pMOS and nMOS of TG cell simultaneously. In this design input B is applied to source of pMOS of GDI/TG cell. Now, for input values of A = 0, B = 0 and A = 0, B = 1, due to inverter before GDI cell, nMOS of GDI cell conducts and it passes strong „0" to output. When A = 1, pMOS of GDI/TG cell and nMOS of TG cell conducts simultaneously, hence input B will appear as output without any degradation ***Vijay Kumar Sharma et all 2020*** Full adder is the heart of ***Jitendra Kumar Saini et all in 2020***,Fast and energy efficient full adder circuit using 14 CNFETs,With the increasing demand for faster, efficient and robust computational devices, the industrial research in circuit design deals with the challenges like size, power, efficiency and scalability. The designers have an array of choices to make use of different design approaches, material or technology to cater to these demands. In recent times, Carbon Nanotube Field Effect Transistor (CNFET) has emerged as an improvised alternative for designing high-speed, low-power and cost-effective circuits. In this manuscript, 1-bit Full Adder circuit (1b-FA) using 14 CNFETs is being proposed in an effort to improve upon the aforesaid characteristics. The design being proposed is simulated with 32 nm CNFET technology at a supply voltage (VDD) of +0.9V using Cadence Virtuoso CAD tool. The performance analysis of various existing full adder designs has been undertaken against proposed design in terms of power, delay and power-delay product (PDP). Parametric variations in CNFET diameter (DCNT) and threshold voltage (Vth) was done for the analysis of output stability. Further, n-bit ripple carry adder (nb-RCA) for (n = 4, 8, 16, 32) was implemented using 1b-FA and compared with the existing nb-RCAs to analyze the performance and efficiency. Later, features like auto fault correction in outputs of 1b-FA were added. ***Dinesh Kumar et all in 2020***,Implementation of parallel computing and adiabatic logic in full adder design for ultra-low-power applications,In this work, the idea of parallel computing for a full adder has been proposed. Based on parallel computing, a new architecture of full adder (A-I) has been proposed in which the input needs to pass through only two transistors to reach the output node which results in reduced delay time. The second design of full adder (A-II) has been proposed with two-phase clocked adiabatic static complementary metal oxide logic which results in decreased power dissipation. The third design of

ISSN(ONLINE):2278 - 3814

full adder (A-III) uses parallel computing for both sum and carry generation. In A-III, a buffer has been introduced to restore the logic level which proves the drive capability of parallel computing logic. The adiabatic logic-based proposed design A-II shows a 61.95% improved power delay product (PDP) as compared to the best-reported body biasing approach-based adder, whereas the fully parallel computing-based design A-III shows a 53.29% improved PDP as compared to double pass transistor-based full adder. Post layout results of the proposed design A-III verified the functionality of proposed parallel computing logic. The proposed designs also perform well under varied temperature conditions. These designs show satisfactory performance at low voltages, whereas the use of adiabatic logic makes these designs energy efficient for low power applications. ***Subodh Wairya et all in 2012,*** presents a comparative study of high-speed and low-voltage full adder circuits. Our approach is based on hybrid design full adder circuits combined in a single unit. A high performance adder cell using an XOR-XNOR (3T) design style is discussed. This paper also discusses a high-speed conventional full adder design combined with MOSCAP Majority function circuit in one unit to implement a hybrid full adder circuit. Moreover, it presents low-power Majority-function-based 1-bit full addersthat use MOS capacitors (MOSCAP) in its structure. This technique helps in reducing power consumption, propagation delay, and area of digital circuits while maintaining low complexity of logic design. Simulation results illustrate the superiority of the designed adder circuits over the conventional CMOS, TG, and hybrid adder circuits in terms of power, delay, power delay product (PDP), and energy delay product (EDP). Postlayout simulation results illustrate the superiority of the newly designed majority adder circuits against the reported conventional adder circuits. The design is implemented on UMC 0.18 m process models in Cadence Virtuoso Schematic Composer at 1.8 V single-ended supply voltage, and simulations are carried out on Spectre S. ***Pankaj Kumar et all in 2016***,Low voltage high performance hybrid full adder, This paper presents a low voltage and high performance 1-bit full adder designed with an efficient internal logic structure that leads to have a reduced Power Delay Product (PDP). The modified NOR and NAND gates, an essential entity, are also presented. The circuit is designed with cadence virtuoso tool with UMC 90-nm and 55-nm CMOS technologies. The proposed adder is compared with some of the popular adders based on power consumption, speed and power delay product. The proposed full adder cells achieve 56% and 76.69% improvement in speed and power delay product metric when compared with conventional C-CMOS full adder. It is also found that the proposed adder cells exhibit excellent signal integrity and driving capability when operated at low voltages.

A. Problem Formulation

The GDI method is a standout amongst the most encouraging logic outline techniques in Adder circuit design. The GDI (Gate Diffusion Input) procedure is a low power rationale plan strategy which empowers usage of an assortment of complex logical capacities utilizing only two transistors PMOS and NMOS combining all four transistors generate EXOR gate. This system is fitting for outline of low power, fast circuits while utilizing few number of transistors (when contrasted with CMOS and other existing methods). The primary inconvenience of the GDI adder is loss of voltage swing which reduces the driving ability of the GDI Adder circuit.

The Pass Transistor Logic (PTL) likewise turns out to be an effective approach to configuration circuits planned for low power applications were minimum no of transistor is required. With the forceful scaling of the transistor estimate because of developing technology, the significance of pass transistor logic has expanded immensely; it is because of the lower hub capacitance acquired in the PTL when contrasted with the node capacitance in CMOS circuit design. The few transistors for the execution ofPTL plans are gotten by quickly diminishing the channel lengths of the transistors. The few parameters which is measured help the transistors in lessening the drop (IR drop) across the circuit. Because of these qualities, PTL union turns into a reasonable rationale plan procedure for doing low power, territory effective outlines to meet the necessities of quickly developing electronic industry.

B. Complementary Metal Oxide Semiconductor Technology in DSM (CMOS)

The ordinary CMOS outline system is the most essential circuit plan procedure in CMOS innovation which has lower power consumption than other technology. This strategy of making CMOS technology by uses two corresponding arrangements of systems to be specific the "pull up" system and " pull down" system the pull up system is made out of PMOS transistor to pass low level signal to charge the load capacitance and the correlative pull down system is made out of the NMOS transistor which help in discharge the system towards ground. The fundamental structure of a plan in the tradition CMOS outline method is appeared in the Fig. 2.1. In the below figure CMOS circuit consist of system of PMOS and NMOS transistors to charge and discharge the output load capacitance, the C-CMOS configuration uses measure up to number of PMOS and NMOS transistors regardless of the necessity of the plan.

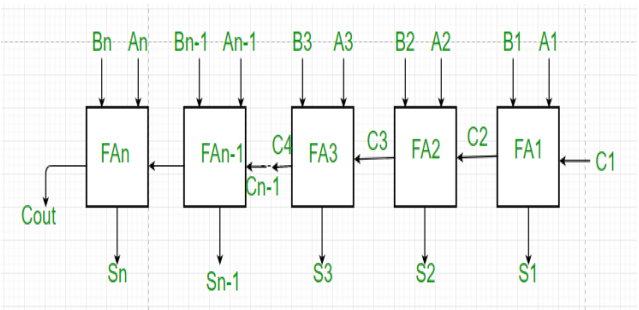

Fig.1: Multiple Full Adder Design

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As the outline recommends the CMOS full adder comprises of 28 transistors with standard CMOS structure both PMOS and NMOS transistor are utilize to form a CMOS structure for saving the power consumption in the circuit, by using this type of technique the voltage swing achieved by the adder circuit is proper. One of its primary benefits is its heartiness against voltage scaling and transistor 28 during scaling of the technology. The correlative plan prompts exceptionally straightforward circuit of a full adder design.

III. METHODOLOGY IN EXISTING ADDERS

The outline of low power with fast digital framework is the prime test for VLSI originators yet a few imperatives dependably exist for the plan of low power frameworks. So one generally needs to make exchange offs to acquire a framework with preferred attributes and numerous choices exist that make exchange offs between speed of the circuit, oxide thickness of transistor, programmability of the device, and different factors which help in improving overall performance of the circuit. Each processor has Arithmetic Logic Unit (ALU) to play out the math operations required to run the process and adder circuit is a basic circuit utilized for all operations which is performed by an ALU of the processor. The mitigation of power dissipation of adder circuit results in overall mitigation of power in ALU block of the processor.

A. Conventional Full Adder Circuit

A full adder is a logical circuit that delivers the expansion of two numbers in a number-arithmetic framework. A one bit full adder circuit addition by using the input A, B, Cin and generate two output known as S and. The full adder comprises of three sources of info (two present bits and one past convey bit) and two yields to be specific whole and convey. Reality table for a full adder circuit is appeared in table I..

Table I. Truth table of full adder circuit design

A	B	C	S_{out}	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

The Boolean operation for full adder outputs can be calculated by using EXOR gate

From the above conditions, which is shown in Fig. 2. For manufacturing full adder circuit we require two XOR gate s, one NAND gate which is minimum number of transistor are used but in Fig.4.1 two AND, OR gate is extra require. This is the most essential type of usage of a adder circuit albeit diverse type of execution is utilized at the circuit level which fluctuates from configuration to plan.

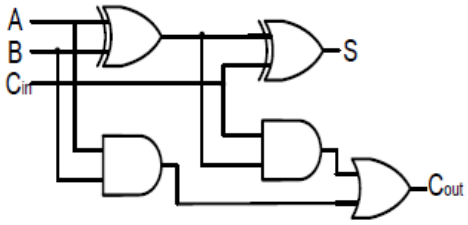


Fig. 2 One Bit Full adder circuit design

IV. SIMULATION AND RESULTS DISCUSSION

All the existing and proposed circuit Schematic is made by using Cadence Virtuoso schematic proofreader apparatus tool. The schematic graphs of XOR and XNOR based full adder circuits have been appeared in Fig. 3 and 4. separately. These schematic graphs of all adder circuits have been planned and recreated at 180nm and 65nm technology having a supply voltage at 1.8V and 1V respectively.

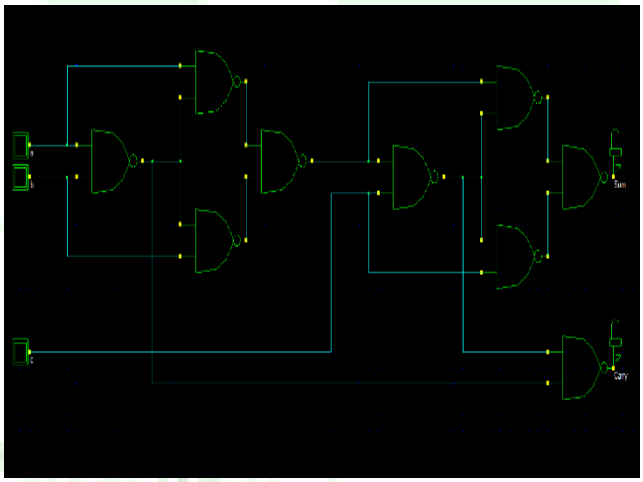
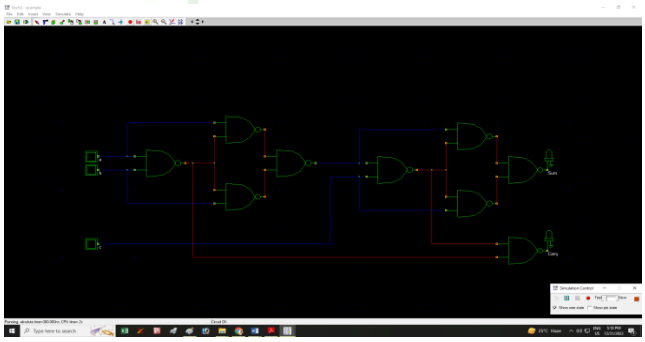


Fig. 3 Full Adder Design



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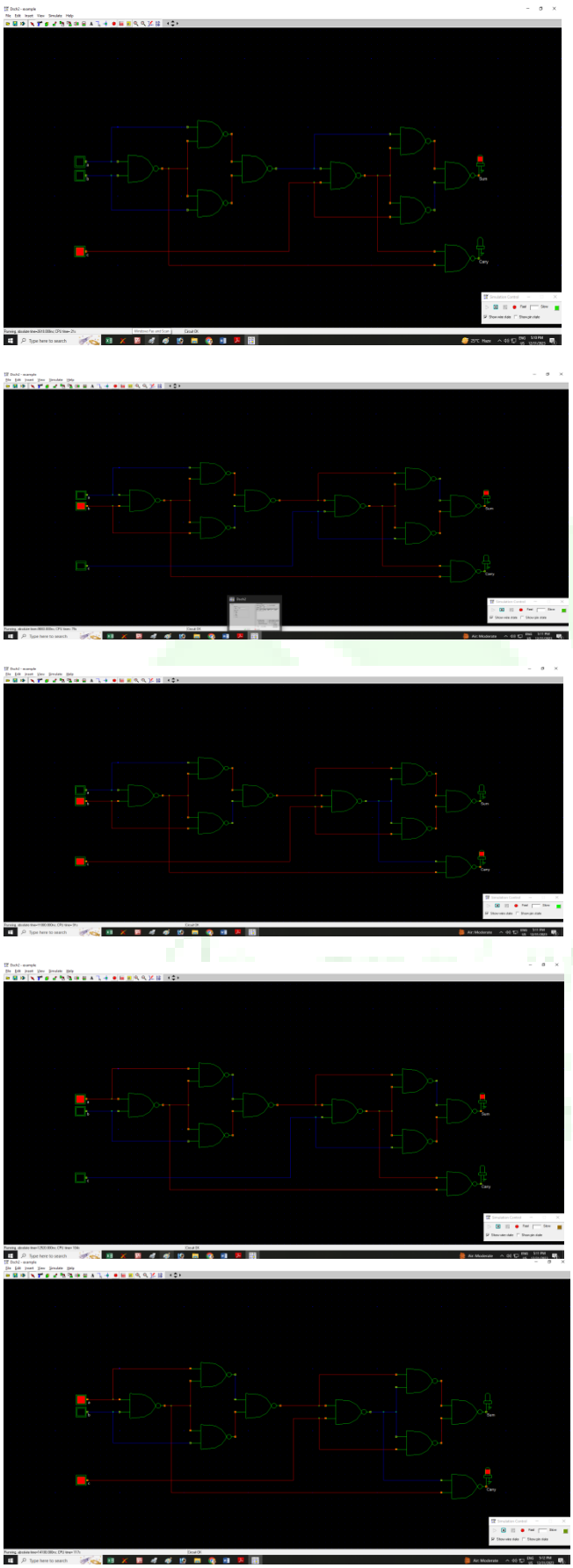

Fig.4: Simulation Result

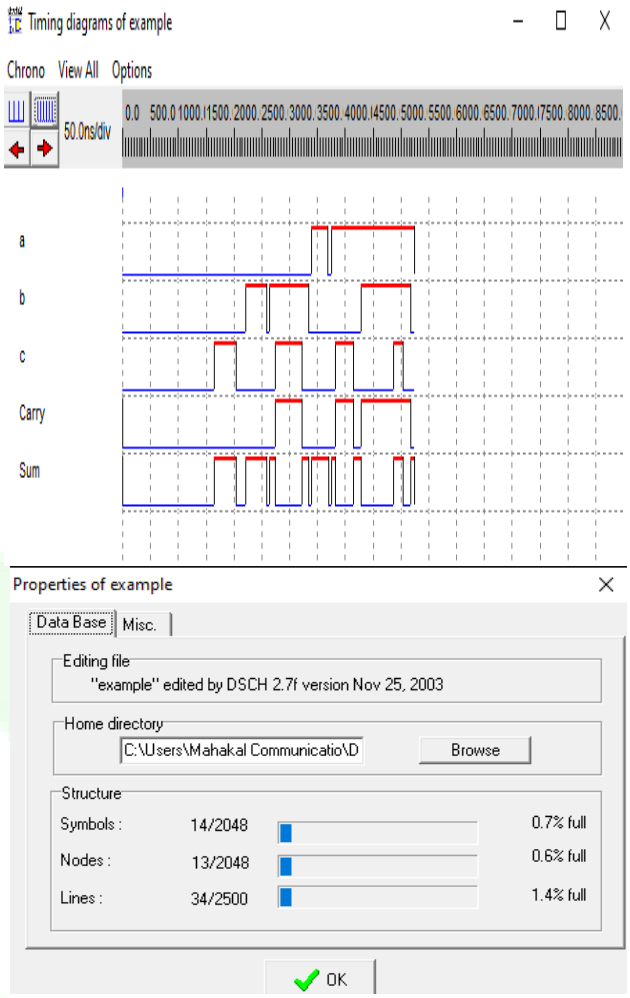

Fig. 5:Simulation Result Waveform Diagram

A. Micro wind Result

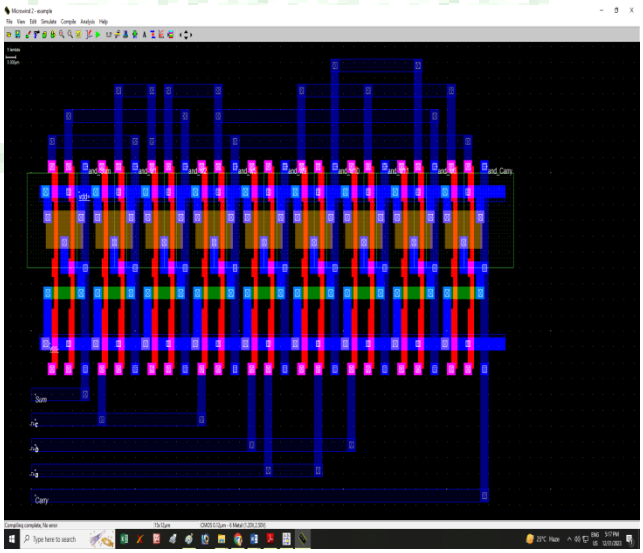

Fig. 6: Micro wind Layout Diagram of Full Adder

Microwind Result at 10ns

Voltege Vs Time Graph:- Volteg Vs Time Graph show in the Figure 5.5. On this simulation power used is

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28.878µw.

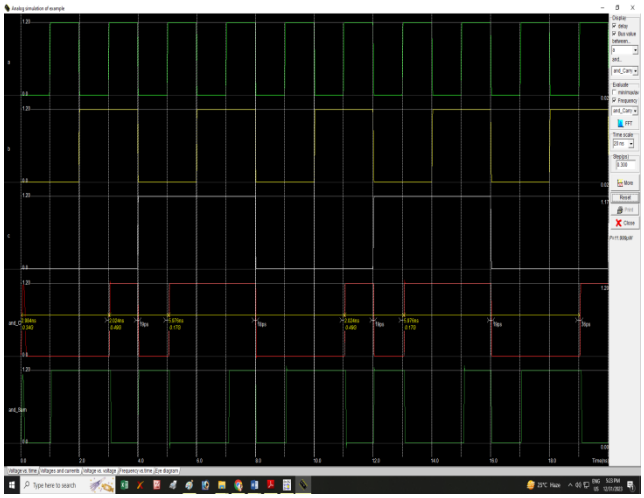

Fig. 7: Voltage Vs Time Graph

Voltege Vs Current Graph:- Voltege Vs Current Graph show in the Fig 8. On this simulation power used is 19.975µw.

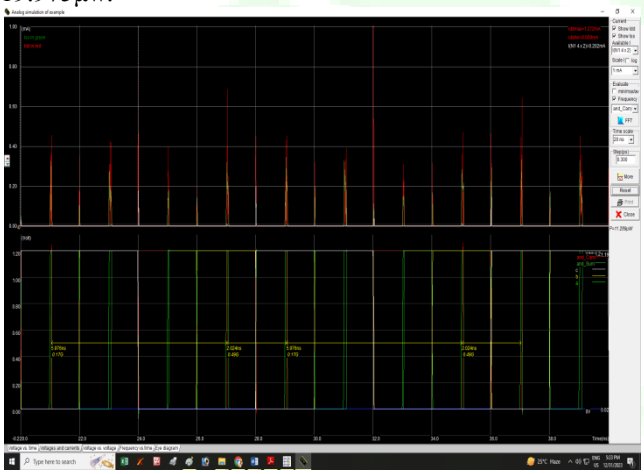

Fig. 8: Voltage Vs Current Graph

Voltage Vs Time Graph:- Voltage Vs Time Graph show in the Fig 9. On this simulation power used is 22.828µw.

Fig. 9: Voltage Vs Time Graph

Frequency Vs Time Graph:- Frequency Vs Time Graph show in the Fig 10. On this simulation power used is 22.828µw.

Fig.10 Frequency Vs Time Graph

Eye Diagram:- Eye Diagram Graph show in the Fig. 11. On this simulation power used is 10.196 µw.

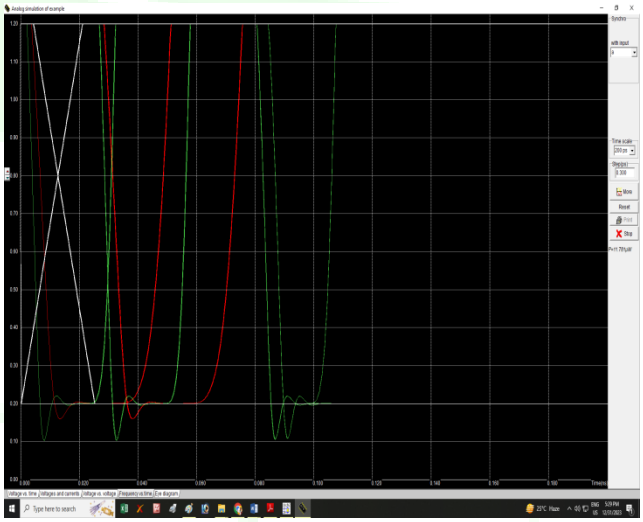

Fig.11: Eye Diagram

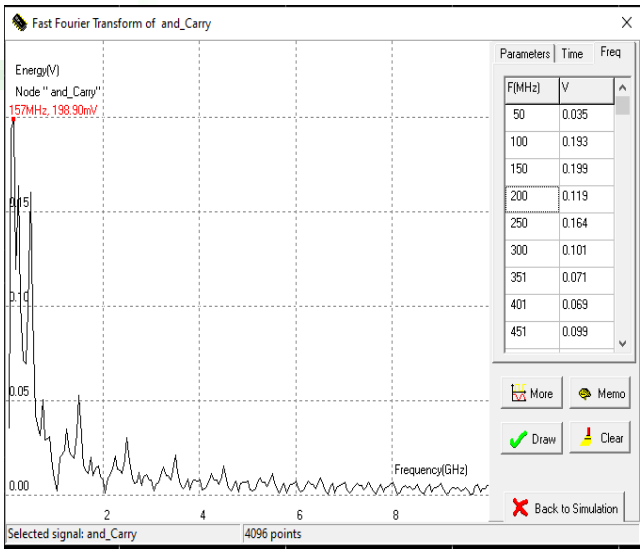

Fig. 12: FFT Analysis of Circuit

V. CONCLUSION

As we discuss in previous chapters for both existing and proposed circuit it is concludes in over both proposed 13T Hybrid GDI full adder circuits shows better performance in terms of lower power consumption in DS Mcircuits, provides lower delay to the circuit and over all there is improvement in Power Delay Product (PDP) than all the existing full adder circuits and proposed XOR and XNOR based circuits which is free from the degradation of the voltage level problem with all the existed circuits when compared with proposed circuit. We have compared all the existing adder circuits with the proposed from the simulation results it is observed that proposed circuits has better performance than other existing adders circuit in terms of power consumption of the circuit, propagation delay of the circuit and overall PDP. In over proposed circuit which is made from XOR single bit GDI hybrid adder circuit which shows maximum saving of power 53.2 % when comparison with existing 16T hybrid adder, maximum reduction propagation delay a maximum of 93.4 % in conventional 28T CMOS adder and the maximum PDP is achieved 96.8% in comparison to conventional 28T CMOS adder while. In proposed XNOR based full adder circuits saves maximum reduction of power upto 56.7 % when compared with to the existing 16T hybrid adder circuit, reduction of delay a maximum of 93.5 % when compared with conventional 28T CMOS adder and maximum saving of PDP upto 97.1 % compared with conventional 28T CMOS adder at lower frequency range upto 100 MHz. As we scale down the technology at 65 nm, The proposed XOR based full adder cell circuits saves the power upto 85.2 % when compared to the existing SERF adder circuit, reduction in delay upto 93.4 % when compared with SERF adder and maximum saving of PDP upto 99 % in comparison to SERF adder. The XNOR based proposed single bit full adder cell circuits produce reduction in power consumption a maximum of 86.8 % in comparison to the existing SERF adder, produces reduction in delay a maximum of 93.7 % in comparison to the SERF adder and a huge reduction in PDP a maximum of 99.2 %in comparison to SERF adder at 100 MHz frequency.

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