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A Implementation and Designing of High Speed Polar Encoder and Decoder for 5th Generation Application

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Abstract:- ***In today's society the ability to communicate with one another has grown, were a lot of focus is aimed towards speed in the telecommunication industry. For transmissions to become even faster there are many ways to enhance transmission speeds of which error correction is one. Padding messages such that they are protected from noise, while using as few bits as possible and ensuring safe transmit is handled by error correction codes. A short code with low complexity is a solution to faster transmission speeds. An error correction code which has gained a lot of attention since its first appearance in 2009 is Polar Codes. Polar Codes was chosen as the 3GPP standard for 5G control channel. The goal of the thesis is to develop and implement Polar Codes and rate matching according to the 3GPP standard 38.212. Polar Codes are then to be evaluated with different block sizes and rate matching settings. Finally Polar Code is compared with Convolutional code in a LTE-simulation environment. The performance evaluations are presented using BLER/(Eb/N0)-graphs. In this thesis a Polar encoder, rate matching and a Polar decoder (with Successive Cancellation algorithm) were successfully implemented. The simulation results show that Polar Codes performs better with longer block sizes and also has a better BLER-performance than Convolutional Codes when given the same message lengths.***

Keywords — 5G control channel, FIFO (First-In First-Out), Successive cancellation decoding (SCD), Turbo Code, Maximum likelihood (ML), Successive cancellation (SC) and Belief propagation (BP)

I. INTRODUCTION

A. Overview of Polar Code

In information theory, a polar code is a straight square error correcting code. The code development depends on a different recursive connection of a short bit code which transforms the physical channel into virtual external channels. At the point when the quantity of recursions turns out to be huge, the virtual channels will in general either have high dependability or low unwavering quality (at the end of the day, they polarize), and the information bits are apportioned to the most solid channels. Polar codes were portrayed by Erdal Arıkan in 2009. There is work proposing this is identical to a prior advanced code for bitwise multistage decoding, a code originally portrayed by Norbert Stolte. It is the principal code with an express development to provably accomplish the channel limit with respect to symmetric paired information, discrete, memoryless channels (B-DMC) with polynomial reliance on the hole to limit. Eminently, polar codes have unobtrusive encoding and decoding multifaceted nature, which renders them alluring for some applications. Moreover, the encoding and decoding vitality unpredictability of summed up polar codes can arrive at the central lower limits for vitality utilization of two dimensional hardware.

The main stage comprises of one radix-2 handling motor (PE2) and onebit FIFO (First-In First-Out). The radix-2 preparing motor is utilized for executing the PE2 activity. Notwithstanding one XOR gate in the PE2, there additionally exist 2 MUXes and basic control circuits. With respect to different stages, the main contrast is the bit length of FIFO. In the n-th stage, FIFO needs 2n-1 bits for the essential information storage. In the comparative way, the radix-4 based Polar encoder plan and contrasted and the radix-2 encoder design, it just requires 2 phases, which each stage comprises of 3 4k - bit of FIFOs and one radix-4 preparing motor (PE4) for a similar 16-point case. The radix-4 preparing motor is answerable for executing the PE4 activity in Fig. 2. Additionally, one PE4 needs 4 XOR gates, the corresponding MUXes, and required control circuits. Because of the normal expansion, the proposed radix-2 and radix-4 encoder structures can be applied for

any intensity of 2 and 4 focuses, separately. Generally important of all, the comparative structure philosophy is summed up to different sorts of radix-k, where k = 8, 16, 32, 64 and so on.

B. TYPES OF POLAR CODE

Attributable to their ability accomplishing performance and low encoding and decoding multifaceted nature, polar codes have drawn a lot of exploration interests as of late. Successive cancellation decoding (SCD) and conviction spread decoding (BPD) are two normal methodologies for decoding polar codes. SCD is successive in nature while BPD can run in equal. Therefore BPD is more alluring for low inertness applications. Anyway BPD has some performance debasement at higher SNR when contrasted and SCD. Linking LDPC with Polar codes is one well known way to deal with improve the performance of BPD, where a short LDPC code is utilized as an external code and Polar code is utilized as an internal code.

C. CRC vs POLAR CODE

For control channel, FAR is the key metric which ought to be fulfilled. FAR relies upon the rundown size and error location capacity of CRC and parity bits. There is sufficient support in writing to check that CRC gives generally excellent performance contrasted with other error recognition codes. CRC is a sort of direct square code, indicating extremely decent error location ability.

D. Advantages Of Polar Code

They have modest encoding/decoding complexity.
As a result they are used for many applications including 5G wireless transmitter/receiver. They are explicit in construction. They are easy to implement due to simple encoding and decoding algorithms. It offers high hardware efficiency. It has helped achieve high throughput in 5G wireless network when used as channel coding. During 5G field trials, Huawei has achieved 27 Gbps.

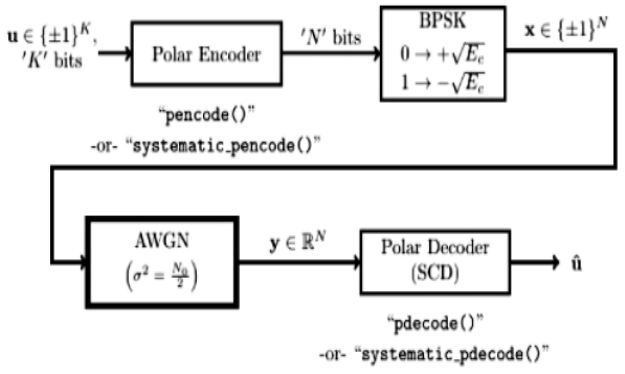

Fig.1: depicts polar coding with polar encoder and decoder modules in a chain.

- Direct polarization & Polar lattices
- Multi-level techniques (Multi-level coding and modulation)
- BICM (Bit interleaved coded modulation)

E. Types of decoders used for polar codes

- Maximum likelihood (ML)
- Successive cancellation (SC)
- Belief propagation (BP)
- List decoder with CRC
- Sphere-decoding

F. Throughput For LDPC Code And Turbo Code

LDPC Code
The throughput of layered BP decoder can be calculated as:

$$Throughput_{[Mbps]} = \frac{L \cdot f_{c[MHz]}}{I \cdot N_{Layer} \cdot \left(\left\lceil \frac{z}{P} \right\rceil + T_{pip} - 1 \right)}$$

Where,
Denotes the number of iteration; i
Denotes the parallelism level; p
Denotes the length of code block without crc; l
Denotes the decoding layer, equals the number of rows for base matrix; layer n
Denotes The Expending Factor; Z
T_{pip} denotes the processing clocks for CNU and VNU updating plus memory reading and writing at each decoding step;
fc denotes the operating frequency.
And, the throughput of flooding decoder with single-frame can be calculated as:

$$Throughput_{[Mbps]} = \frac{L \cdot f_{c[MHz]}}{I \cdot (N_{Layer} + T_{pip} - 1)}$$

G. Turbo Code

The throughput of turbo MAP decoder can be calculated as:
Where,
I denotes the number of iteration;
P denotes the parallelism level;
L denotes the length of code block without CRC;
W denotes the number of extra trellis for MAP decoder;
a denotes the number of bits processed in one MAP core per clock cycle, i.e. 1 for Radix-2 and 2 for Radix-4.
fc denotes the operating frequency.
The parameters of LDPC & Turbo code for throughput depicted in Figure 2 are shown in the table I.

Table I: The Parameters of LDPC & Turbo Code For Throughput

LDPC		Turbo	
I	10 for layered decoder, 20 for flooding decoder	I	4
P	1024	P	1024
L	8192	L	8192
N_{layer}	[16 12 10 8 6 4] for code rates of [1/3,2/5,4/9,1/2, 4/7,2/3]	W	[32 64 128] for low, medium and high code rates respectively
z	1024	a	1
T_{pip}	4	f_c	400 MHz
f_c	400 MHz		

II. LITERATURE REVIEW

B. Chen et al.,[1] Physical unclonable capacities (PUFs) are generally new security natives utilized for gadget confirmation and gadget explicit mystery key age. In this work we center around SRAM-PUFs. The SRAM-PUFs appreciate uniqueness and randomness properties coming from the inborn randomness of SRAM memory cells, which is an aftereffect of assembling varieties. This randomness can be converted into the cryptographic keys along these lines dodging the need to store and deal with the gadget cryptographic keys. Therefore these properties, joined with the way that SRAM memory can be frequently found in the present IoT gadgets, make SRAM-PUFs a promising candidate for making sure about and verification of the asset compelled IoT gadgets. PUF perceptions are constantly influenced by commotion and natural changes. Therefore mystery age plans with aide information are utilized to ensure solid recovery of the PUF-based mystery keys. Error correction codes (ECCs) are a fundamental piece of these plans. In this work, we propose a viable error correction development for PUF-based mystery age that depend on polar codes. The subsequent plan can create 128-piece keys utilizing 1024 SRAM-PUF bits and 896 aide information bits and accomplish a disappointment likelihood of 10^{-9} or lower for a down to earth SRAM-PUFs setting with bit error likelihood of 15%. The strategy depends on successive cancellation joined with list decoding and hash-based checking that utilizes the hash that is as of now accessible at the decoder. Moreover, a versatile rundown decoder for polar codes is investigated. This decoder expands the rundown size just if necessary.

D. Chen et al.,[2] In this work we investigate physical (PHY) layer message validation to battle enemies with limitless computational limit. In particular, a PHY-layer verification framework over a wiretap channel (W1,W2) is proposed to accomplish information-theoretic security with a similar key. We build up a theorem to uncover the prerequisites/conditions for the verification framework to be information-theoretic secure for verifying a polynomial number of messages as far as n. In view of this theorem, we plan a validation convention that can ensure the security necessities, and demonstrate its confirmation rate can move toward endlessness when n goes to interminability.

D. Chen, N. Cheng et al.,[3] In this work we investigate multi-message verification to battle enemies with limitless computational limit. A validation framework over a wiretap channel (W 1 , W 2) is proposed to accomplish information-theoretic security with a similar key. The proposed framework connects the two examination zones in physical (PHY) layer security: secure transmission and message confirmation. In particular, the sender Alice initially transmits message M to the recipient Bounce over (W 1 , W 2) with an error correction code; at that point Alice utilizes a hash work (i.e., ε-AWU 2 hash capacities) to produce a message label S of message M utilizing key K, and encodes S to a codeword X n by utilizing a current firmly secure channel coding with exponentially little (in code length n) normal likelihood of error; at long last, Alice sends X n over (W 1 , W 2) to Weave who confirms the got messages. We build up a theorem with respect to the prerequisites/conditions for the verification framework to be information-theoretic secure for confirming a polynomial number of messages. In light of this theorem, we propose and execute a proficient and possible validation convention over twofold symmetric wiretap channel (BSWC) by utilizing Straight Criticism Moving Register based (LFSR-based) hash capacities and solid secure polar code. Through broad trials, it is exhibited that the proposed convention can accomplish low time cost, high validation rate, and low confirmation error rate.

III. POLAR ENCODER AND DECODER

Polar codes are a channel coding innovation and all channels coding innovation works in essentially a very comparative way. Correspondence joins are defenseless to errors because of random clamor, impedance, gadget debilitations, and so on that corrupt the original information stream at the less than desirable end. Channel coding essentially utilizes a lot of algorithmic procedure on the original information stream at the transmitter, and another arrangement of procedure on the got information stream at the recipient to correct these errors. In channel coding wording, the whole of these activities at the transmitter and recipient are separately meant as encoding and decoding tasks. Channel coding techniques comprehensively fall under two classes: square codes and convolutional codes. Square codes work on a square of information/bits with fixed estimate and apply the control to this square at the transmitter and beneficiary. Reed-Solomon codes, generally utilized on the hard plates of PCs, are one case of this sort of code. Convolutional codes, then again, work on floods of information with more arbitrary quantities of information/bits. These codes apply a sliding window technique that gives a generous decoding advantage. Straightforward Viterbi codes are a case of this kind of code.

Table II: Requirements of coding and modulation in the three scenarios of NR

KPIs	eMBB	mMTC	URLLC
Performance	Good performance at all TBS and MCS, especially large TBS No error floor at BCER=10^{-3}	Good performance at small TBS No requirement of error floor	Good performance at small TBS No error floor at BCER=10^{-5}
Complexity	Low	Very Low	Middle
Latency	Low	Large	Low
Throughput	High Highest peak rate with 20 Gbps	Low	Low
Power consumption	Middle	Low	Middle
User number	Middle	High	Low
Flexibility of mother code rates	multiple rates from 1/3 to 0.9	multiple rates from 1/3 to 0.9	multiple rates from 1/5 to 0.9
Flexibility of TBS	TBS from 40 to X thousands	TBS from 40 to X thousands	TBS from 20 to 1000
HARQ function	Yes	Yes	Yes

As you would speculate, impressive profitable examination has been done throughout the years into the link of square and convolutional codes to consolidate the advantages of both. For instance, the RSV code, which was the best performing code until turbo codes, was a mixture of the Reed-Solomon code, which is a square code, with a Viterbi convolutional code.

A. Turbo Code

Turbo coding is a case of a connected code strategy. The performance gains contrasted with other such codes are incredibly immense. They were the primary arrangement of codes to move toward the Shannon limit with a generally moderate degree of multifaceted nature. Turbo codes consolidate two convolutional type encoders, two sequential decoders and an interleaver. Turbo codes get their name from the novel criticism circle they utilize that, adroitly, in any event looks like a similar component by which turbo fumes frameworks work in vehicles. The genuine development in turbo codes lies in the smarts encompassing how delicate information is utilized. Prior frameworks required hard information about the bits (for example 0's or 1's) being gotten. Be that as it may, turbo codes just require a probabilistic proportion of each bit to be decoded correctly.

IV. PROPOSED METHODOLOGY

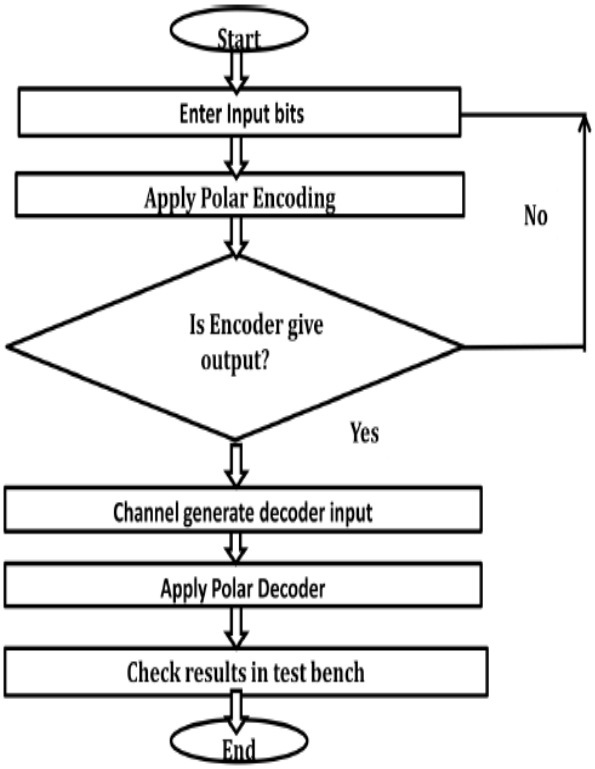

Fig.2 : Flow Chart

Polar Code is a new efficient coding technology; it is the first channel coding method that can be strictly proven to achieve channel capacity. Polar code as a high-performance error correction code technology, its huge application potential has also cause a strong concern among 5G standardization of communications research and development institutions and academic word. In the case of channel combining and channel separation, channel polarization occurs. The focus of channel coding research may be stated quite simply: develop high performance channel codes that mitigate the effect of the errors in a communication link (bit-error-rate is the common performance measure used here).

Step-1: Assign input bits into polar encoder and it give encoder output.

Step-2: Encoder output applies in channel and it generates decoder input.

Step-3: This input applies in decoder and it generates decoder output, this is same as assigned input.

Step-4: Now check all results in test bench and calculate all parameters.

V. IMPLEMENTATION AND RESULTS

A. Software Details

Xilinx ISE (Coordinated Blend Condition) is a thing instrument made by Xilinx for mix and assessment of HDL structures, enabling the authority to incorporate ("gather") their game plans, perform timing assessment, investigate RTL charts, reproduce a course of action's response to various upgrades, and organize the objective contraption with the item engineer.

Xilinx ISE is a course of action condition for FPGA things from Xilinx, and is unequivocally coupled to the structure of such chips, and can't be utilized with FPGA things from different dealers. The Xilinx ISE is in a general sense utilized for circuit amalgamation and structure, while ISIM or the Model Sim reason test framework is utilized for framework level testing. Different parts dispatched with the Xilinx ISE incorporate the Presented Progress Pack (EDK), a Thing Improvement Unit (SDK) and ChipScope Star.

Simulation

Framework level testing might be performed with ISIM or the Model Sim strategy for thinking test framework, and such test ventures should moreover be formed in HDL vernaculars. Test seat undertakings may incorporate mirrored info signal waveforms, or screens which watch and attest the yields of the contraption under test. Model Sim or ISIM might be utilized to play out the going with sorts of preoccupations.

Synthesis

Xilinx's made sure about figurings for amalgamation engage plans to keep approaching 30% speedier than doing combating ventures, and allows more obvious explanation thickness which decreases experience time and expenses. Moreover, considering the expanding multifaceted nature of FPGA surface, including memory squares and I/O squares, more marvelous blend calculations were made that different pointless modules into cuts, decreasing post-position goofs.

RTL VIEW OF PROPOSED DESIGN

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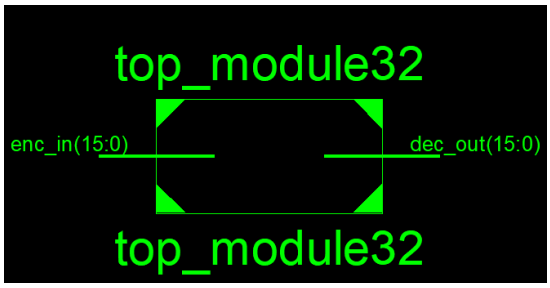

Figure 3: Top view of proposed model

In figure 3 showing top level of proposed polar code model. Here apply 16 bit input and after complete process it gives 16 bit output.

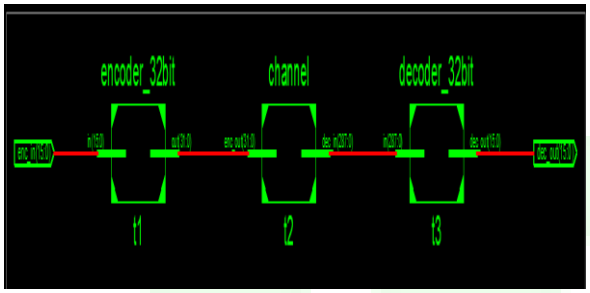

Figure 4: Complete process of proposed model

Figure 4 presenting complete process block diagram in form of RTL view. Here it is clear that all process divide in three steps. The details of all process is explain step via step in below diagrams.

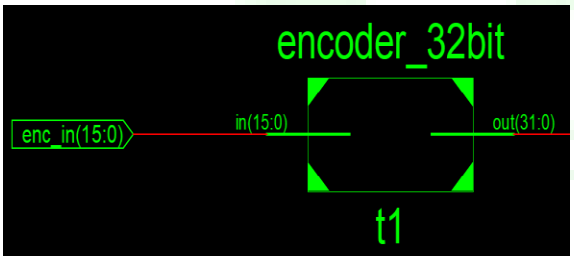

Figure 5: Encoder of proposed model

In figure 5 showing encoder stage of proposed model, here apply 16 bit input and it generate 32 bit output after add encoding bits.

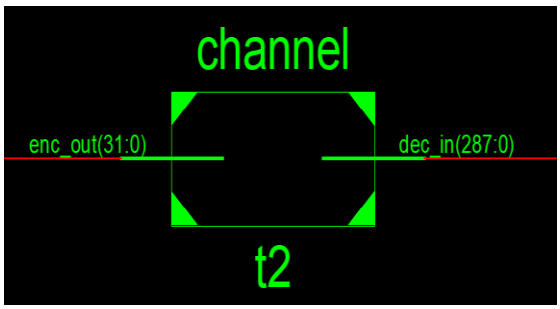

Figure 6: Channel of proposed model

In figure 6 showing channel stage of proposed model, here apply 32 bit encoder output and it generate 288 decoder input bit after add 9 bit for each encoder bit, it also called frozen bit.

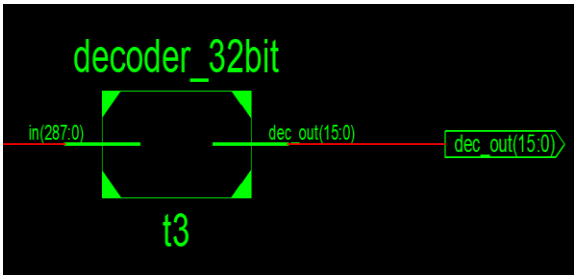

Figure 7: Decoder of proposed model

In figure 7 showing decoder stage of proposed model, here apply 288 decoder input bit and it generate 16 bit output on the other hand recover original data.

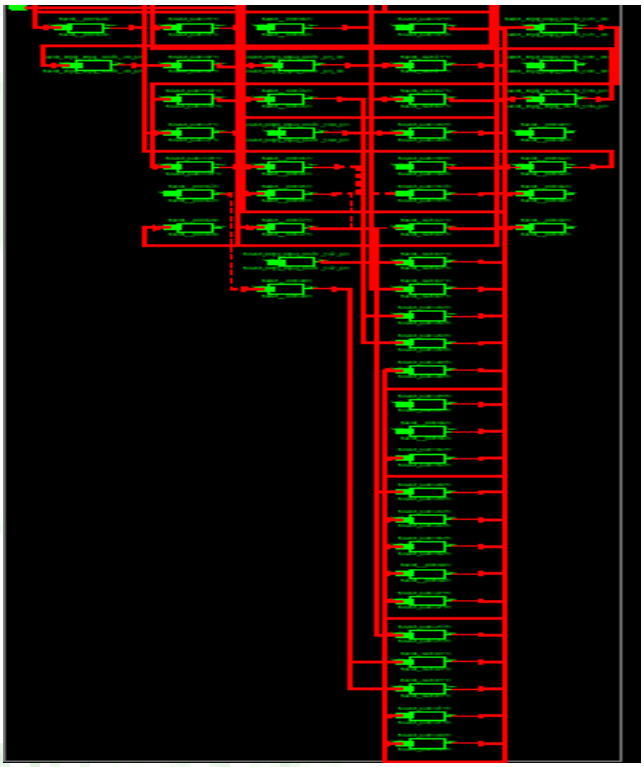

Figure 8: RTL view of proposed model

Figure 8 showing register transfer level diagram which contain all blocks and wires.

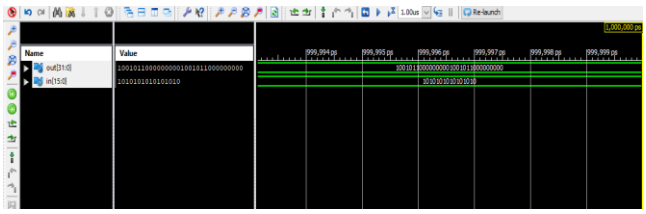

Figure 9: Test bench result at encoder

Figure 9 showing result in test bench, here apply 16 bit input that is 1010101010101010. After encoding it generate 1001011000000000010010110000000000.

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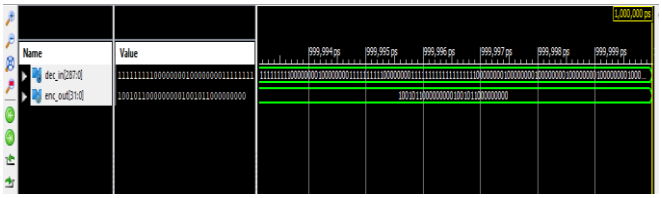


Figure 10: Result at channel

Figure 10 showing channel result in test bench, here apply 32 bit encoder output that is 10010110000000001001011000000000. It generates 288 decoder input bit that is hff80403ff00ffffe01008040201008040201ff80403ff00ffffe 01008040201008040201 in hexa decimal.

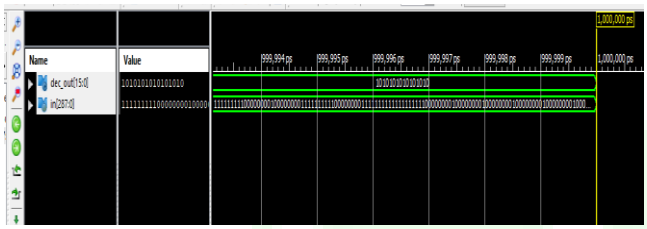


Figure 11: Result at decoder

In figure 11 showing decoder stage of proposed model in test bench, here apply 288 decoder input bit 288 decoder input bit that is hff80403ff00ffffe01008040201008040201ff80403ff00ffffe 01008040201008040201 and it generate 16 bit output 1010101010101010on the other hand recover original data.

Figure 12: Test bench result verification

Finally figure 12 showing input and output bits at same test bench that is 1010101010101010 apply at encoder and at decoder again receive 1010101010101010.

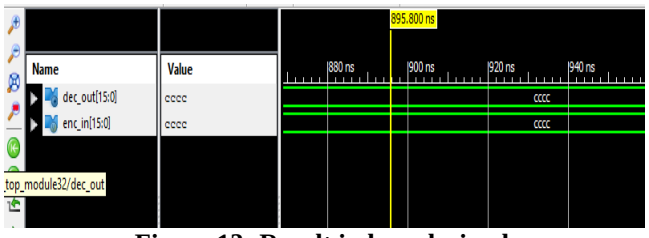


Figure 13: Result in hexadecimal

Figure 13 showing result in hexadecimal, here encoder input is cccc and decoder output is also cccc.

Table III: HDL Synthesis Report

Parameter	Value
# Adders/Subtractors	400
8-bit adder	320
9-bit adder	80
# Comparators	80
8-bit comparator less	80
# Xors	149
1-bit xor2	138
1-bit xor3	9
1-bit xor4	1
1-bit xor5	1

Table IV: Advanced HDL Synthesis Report

Parameter	Value
# Adders/Subtractors	388
8-bit adder	388
# Comparators	80
8-bit comparator less	80
# Xors	149
1-bit xor2	138
1-bit xor3	9
1-bit xor4	1
1-bit xor5	1

Table V: Design Statistics

Cell Name	Numbers
# IOs	32
# BELS	2200
# GND	1
# INV	1
# LUT1	1
# LUT2	112
# LUT3	96
# LUT4	264
# LUT5	302
# LUT6	608
# MUXCY	393
# MUXF7	32
# VCC	1
# XORCY	389
# IO Buffers	32
# IBUF	16
# OBUF	16

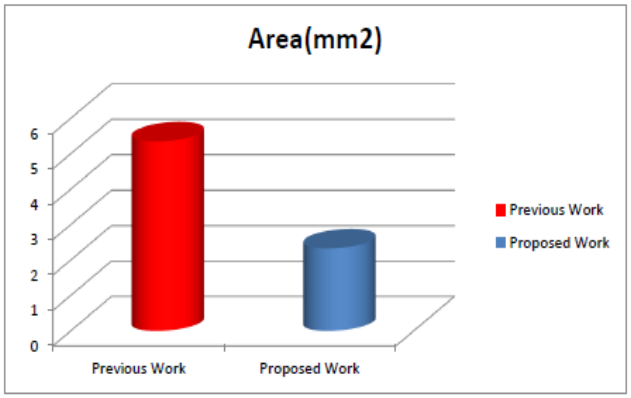
Table VI: Device utilization summary

Selected Device :	5vlx110tff1136-1
Number of Slice LUTs:	1384 out of 69120 2%
Number used as Logic:	1384 out of 69120 2%
Number of LUT Flip Flop pairs used:	1384
Number with an unused Flip Flop:	1384 out of 1384 100%
Number with an unused LUT:	0 out of 1384 0%
Number of fully used LUT-FF pairs:	0 out of 1384 0%
Number of bonded IOBs:	32 out of 640 5%
Delay	139.612ns (32.713ns logic, 106.899ns route) (23.4% logic, 76.6% route)
Total REAL time to Xst completion:	31.00 secs
Total CPU time to Xst completion:	30.48 secs

Table VII: Simulation Parameter and Comparison with previous work

Sr No.	Parameter	Previous Work	Proposed Work
1	Method	Polar decoder	Polar encoder and polar decoder
2	Area	5.35 mm^2	2.33 mm^2
3	Delay	1534ns	139.612ns
4	Power	1072.9 mW	43mW
5	Time	NA	30.48 secs
6	PDP	164153	6003

Table VII showing comparison of proposed work with previous work, so it can be seen that proposed work gives better result than existing work.



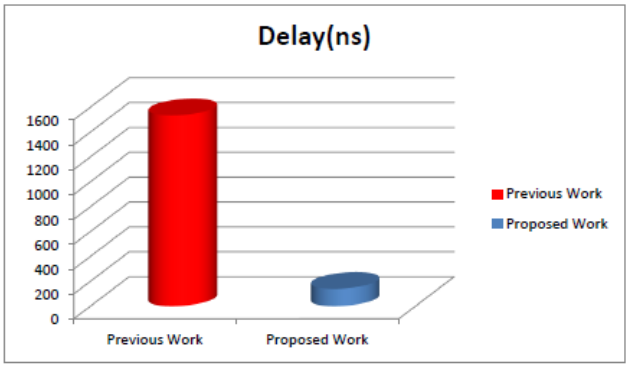


Figure 14: Comparison of delay

From figure 13 and 14, it is clear that proposed polar encoder and decoder gives significant performance improvement. Although 5G communication and application is still in testing phase and this research provide encoding and decoding scheme under proposed constraints

VI. CONCLUSION

In this work investigated the best in class in polar code in encoding and decoding form. It was demonstrated that the many decoding algorithms were created and actualized to address different application prerequisites. Additionally contrast polar code and CRC code. Numerous scientists recommend that polar code can be utilized ahead of time remote correspondence for people to come. In this work, we have nitty gritty the polar code encoding process inside the fifth era remote frameworks standard, furnishing the peruser with an easy to use depiction to understand, execute and recreate 5G-agreeable polar code encoding. This encoding chain grandstands the fruitful efforts of the 3GPP standardization body to meet the different prerequisites on the code for the eMBB control channel: low depiction multifaceted nature and low encoding intricacy, while covering a wide scope of code lengths and code rates. Throughout this work, we implied that the standardization procedure additionally considered the recipient side. Normal for current channel coding, the encoder was structured to such an extent that the decoder can be executed with achievable multifaceted nature and work at the necessary idleness, expecting best in class decoders and equipment. New decoding standards or decoding models, nonetheless, may now be created so as to enhance decoding multifaceted nature or likewise increment error-rate performance. With the 5G eMBB control channel, polar codes have discovered their first appropriation into a standard just 10 years after their creation.

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