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A Literature Review on Different Binary Operation Using Different Booth Algorithms

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***Abstract*—In this survey work focus on advancements in manufacturing and designing capabilities allows world to placing a complete embedded system on a single chip. With these improvements it becomes possible to design a system or a complete work model as a mix of software simulation and running on one or more generic processors and specialized and customized hardware. In this survey paper discuss the different booth multiplier and its architecture that is used in low power devices. In the last decade there are different multiplier introduced that is used to increase the efficiency of the circuit and "true power minimization". For the reduction of power researchers are focus on system level architecture optimization (outer loop), block level optimization (intermediate loop), and fixed topology optimization (inner loop). In this survey paper discuss the different methods and its advantages and disadvantages. Low Power VLSI circuit has become important criterion for designing the energy efficient electronic designs for high performance and portable devices. In the majority of DSP application the critical operations are the multiplication. For the performance evaluation of this work check its power consumption.**

Keywords*— *Low-power multiplier, Quaternary Carry Increment Adder (QCIA), Area-efficient design, High-speed arithmetic, Digital circuits, Low-power VLSI, Quaternary logic etc.

I. INTRODUCTION

An increase of half-hearing person caused by progressive aging of society in our country leads to an increase in demand for a digital hearing aid which includes a digital signal processor (DSP). There is a hard physical limit for battery capacity which stems from its wearing form. So the battery life of an existing digital hearing aid comes up to only about few days [1]. To solve the problem for the battery life of a digital hearing aid, there are a few approaches to achieve lower driving voltage for an analog amplifier inside a hearing aid [2]. However, the analog circuit is significantly affected by external noise under low voltage environment. In recent, it is popular to develop AD/DA converter and DSP with low power consumption oriented to a digital hearing aid [3]. Since most of digital signal processing can be reduced to the multiply-accumulate operation, DSP incorporates a multiply accumulator (MAC) which can compute sum of product efficiently. The multiplier, which MAC consists of, requires much cost for calculation time and circuit area compared with the accumulator. Thus the performance of DSP is highly dependent on the performance of multiplier. Due to recent development of a micro integrated circuit, the multiplier generally is implemented as a parallel multiplier with O(n2) full adders (FA) for n-bit input vectors. In terms of the band frequency, the human ear can hear sounds as low as 20 Hz up to 20,000 Hz. So the parallel multiplier has too high working frequency to implement DSP oriented to a hearing aid. A serial multiplier, which repeatedly performs addition operation to carry out multiplication, has lower working frequency but has smaller circuit area relative to the parallel multiplier and can achieve low power consumption. Several studies are reported which apply serial multiplier to implement DSP of a hearing aid [4]. Serial multiplier can be generally classified into word-serial multipliers implemented by using an n-bit adder and bit-serial multipliers [5] implemented by a single full adder Connectivity). Day by day IC technology is getting more complex in terms of design and its performance analysis. A faster design with lower power consumption and smaller area is implicit to the modern electronic designs. Unceasing advancement in microelectronics design technology makes improved use of energy, encrypt data successfully, communicate information much more steadfastly, etc. Particularly, many of these technologies address low-power consumption to meet the requirements of various portable applications. In

these application systems, a multiplier is a fundamental arithmetic unit and widely used in circuits, for which the multiplication process should be optimized properly. Multipliers generally have extended latency, huge area and consume substantial amount of power. Hence low-power multiplier design has become an important part in VLSI system design. Everyday new approaches are being developed to design low-power multipliers at technological, physical, circuit and logic levels.

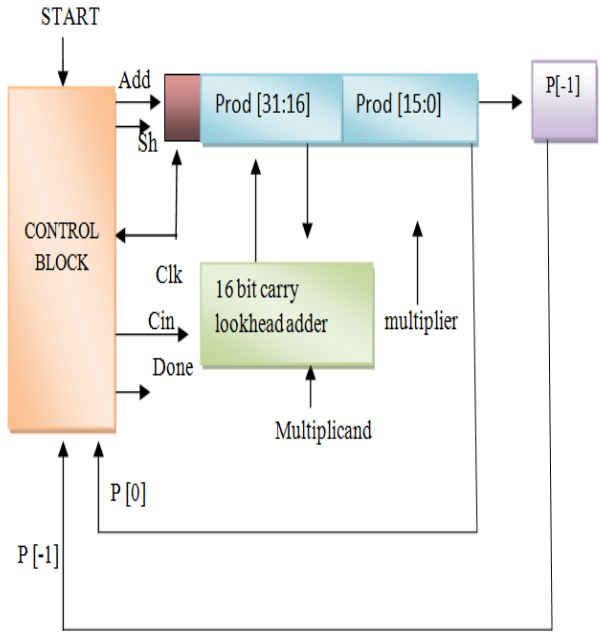

Fig. 1 Shows Structure of booth multiplier

Since the multiplier is generally the slowest element in a system, the system's performance is determined by performance of the multiplier. Also multipliers are the most area consuming entity in a design. Therefore, optimizing speed and area of a multiplier is a major design issue nowadays. However, area and speed are usually conflicting constraints so that improving speed results in larger areas and vice-versa. Also area and power consumption of a circuit are linearly correlated. So a compromise has to be done in speed of the circuit for a greater improvement in reduction of area and power.

II. BASIC ALGORITHM FOR BINARY MULTIPLICATION

A Binary multiplier is an electronic device used in digital electronics or in a computer or other electronic devices to carry out multiplication of two numbers depicted in binary format. It is built using binary adders. The most basic technique involves generating a set of partial products, and then summing the partial products simultaneously. This process is similar to the method which is taught to lower classes' students in school for conducting long multiplication on base-10 integers, but has been modified here for application to a base-2 (binary) numeral system.
The rules for binary multiplication are stated as given:

1. If the multiplier digit is 1, the multiplicand is copied down and it gives the product.
2. If the multiplier digit is 0 then we get a product which is also 0.

For designing such a multiplier circuit we should have the circuitry to carry out or do the following four things:

1. It should be capable of recognizing whether a bit 0 or 1 is.
2. It should be capable of shifting the left partial product.
3. It should be capable of adding all the partial-products to give the product as a sum of the partial products.
4. It should examine sign bits and if they are similar, the sign of the product will be a

Positive representation and if the sign bits are opposite then the product will be negative. The sign bit of the product which has been stored with the above criteria should be displayed along with the product.

III. LITERATURE SURVEY

Kapil Juneja et.al (2025) Altering a single hardware component may significantly impact the system's claimed performance, power consumption, and concurrent functioning. The multiplier is a fundamental component of these digital circuits and systems. Carry look-ahead (CLA) adducts are low-power components used by researchers, including numerous advancements to minimize latency and power consumption. The Baugh Wooley multiplier is a prominent multiplier that integrates Carry Lookahead Adder (CLA) technology. This study presents an improved design for the multiplier. This study enhanced the structural performance of the Baugh-Wooley Multiplier by integrating a carry look-ahead adder using Quaternary logic. This design used the Wallace Tree method to enhance functionality. This suggested enhanced Baugh-Wooley multiplier, designed for 180 nm technology, requires just 1.8 watts of power. The suggested design is contrasted with the CLA Multiplier, QSDCLA (Quaternary Signed Digit-based Carry Look Ahead) Multiplier, Baugh-Wooley Multiplier, Wallace Tree Multiplier, Hasan Multiplier, and Improved Radix Adder. We used delay and energy consumption as our evaluative measures. The latency was decreased to 0.0008962 ns, and power consumption was reduced by 1.693 W using the suggested design. The findings indicate that the new multiplier is much more effective and dependable than its predecessors [01].

Rajashri R. Korde et.al (2024) Arithmetic circuits are essential in both generic and application-specific procedural circuits. Multiple Valued Logic (MVL) offers a crucial advantage regarding future density per circuit space in comparison to traditional binary logic. Quaternary (four-valued) logic provides the advantageous feature of seamless integration with binary logic, since base four (2^2) facilitates the implementation of straightforward encoding and decoding circuits. The intentional entirety is shown using a collection of fundamental quaternary cells. The cell library facilitated the Supplementary Symmetrical Logic Circuit Structure (SUSLOC) unit of measurement, which was constructed, simulated, and used to construct

various quaternary fixed-point arithmetic circuits, such as adders and multipliers. These SUSLOC circuit cells serve as a unit of measurement for acceptable SPICE models, as well as for arithmetic structures that adhere to valid practices. System Verilog models for intentional accuracy. The concepts of quaternary (radix-4) twin amount secret writing serve as a unit of measurement to enhance the power and performance of adder circuits using prevalent CMOS gate technology [02].

Daniel Etiemble et.al (2023) The ordered collection of ternary values (0 < 1 < 2) suggests utilizing Post algebras. Implementing ternary circuits is best using monotonic Post algebra. For a completely ordered collection of values, deconstruct ternary values into binary values using threshold decoders and encode the binary values back into ternary values. Use of binary calculation in ternary circuits is inevitable. Contrasting methods for implementing ternary adders have been described: The naïve technique splits A and B ternary inputs into binary Ai and Bi, with Ai/Bi=2 when A/B=i and 0 otherwise. A0, A1, A2, B0, B1, B2 are used to calculate the binary outputs of S0, S1, and S2. The final encoder calculates Te ternary sum from S0, S1, S2, and Cin. The output carry is calculated using the same method. The MUX-based technique restricts ternary-to-binary and binary-to-ternary encoding to A^1 and A^2 functions, where $A^1=(A+1) \bmod 3$ and $A^2=(A+2) \bmod 3$. In step 10, multiplexers transfer ternary values A, A^1, and A^2 to the output total based on B and Ci values. The carry output is calculated using threshold decoder outputs and multiplexers. MUX-based method beats naïve. All ternary adders proposed in the last decade include these two opposing techniques. The suggested and simulated MUX-based ternary adder is likely comparable to the best [03].

K Gavaskar et.al (2023) This article presents a Carry Increment Adder using the QSD number system to substitute the Quaternary Carry Look Ahead Adder in an array multiplier circuit. In VLSI, power consumption, latency, and area are the determinants of design efficiency. The Tanner EDA tool with 250 nm technology is used for circuit simulation, and the aforementioned analyses are conducted. The studies are conducted for the current Quaternary Carry Look Ahead Adder multiplier, and the results are compared. The QSD provides carry-free addition, hence reducing the carry propagation latency seen in binary arithmetic. This improves the velocity of the Quaternary Carry Increment Adder. The Quaternary Carry Increment Adder has reduced power consumption and consumes less room compared to the current approach. This is due to the fact that the suggested technique incorporates fewer transistors than the current Quaternary Carry Look Ahead Adder multiplier. The findings indicate that the suggested technique achieves a 12.57% reduction in PDP, demonstrating its superior efficiency. In future endeavors, the dimensions of the developed circuits may be enhanced [04].

Jenila R et.al (2022) In digital systems, power and energy consumption are critical restrictions, and multiplication is the primary operation that often employs mathematical modules. The preceding parallel decimal multiplication analysis emphasizes two primary factors: latency and area of these mathematical modules, and suggests potential solutions. This study introduces a prediction-based approach that is low in comparison to previously obtained findings. The power addition approach used to enhance decimal multiplication consumes significant energy and illustrates its impact on multiplier design. The experiment findings indicate an 11.5 percent increase in efficacy and a 10.13 percent reduction in total power consumption regarding energy utilization. An efficient method may be further built to minimize power consumption and latency [05].

IV. BOOTH'S ENCODING

Booth's encoding or Booth's multiplication algorithm [1] is a multiplication algorithm which can multiply two signed binary numbers in a two's complement notation. Booth's algorithm has the ability to perform fewer additions and subtractions in comparison to normal multiplication algorithm. It is an encoding process which can be used to minimize the no of partial products in a multiplication process. It is based upon the relation

$$2n = 2n+1 - 2n$$

Shift and Add Multiplication

A standard approach discussed by Yuke Wang et al [08] could perform multiplication by "shift and add", or normal "long multiplication". That is, for each column in the multiplier, shift the multiplicand to the appropriate number of columns and multiply it by the value of the digit in that column of the multiplier, to obtain a partial product. The partial products are then added to obtain the final result. Figure 2 shows the basic block diagram for shift and add multiplication. With this system, the number of partial products tallies exactly with the number of columns in the multiplier**. [08]**

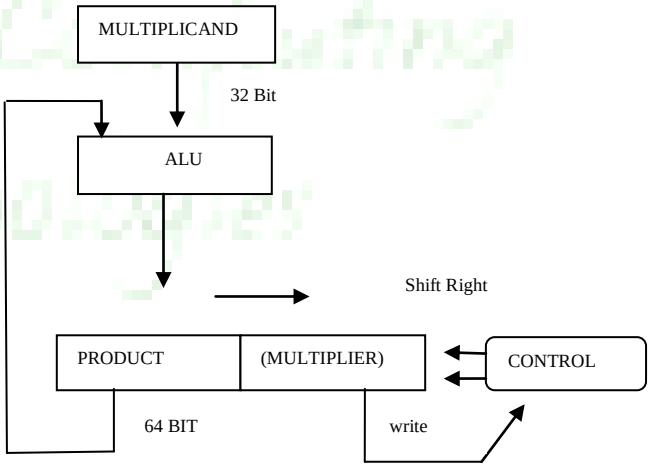

Fig. 2 Shift And Add Multiplication

Booth Multiplication Algorithm

One of the solutions for realizing high speed multipliers is to enhance parallelism which helps in decreasing the number of subsequent calculation stages. The original version of Booth's multiplier (Radix – 2) had two drawbacks. The number of add / subtract operations became variable and hence they became inconvenient

while designing Parallel multipliers. The Algorithm becomes inefficient when there are isolated 1s. These problems are overcome by using Radix 4 Booth's Algorithm which can scan strings of three bits with the algorithm given below. The design of Booth's multiplier in this work consists of four Modified Booth Encoders (MBE), four sign extension correctors, four partial product generators (comprises of 5:1 multiplexer) and finally a Wallace Tree Adder.

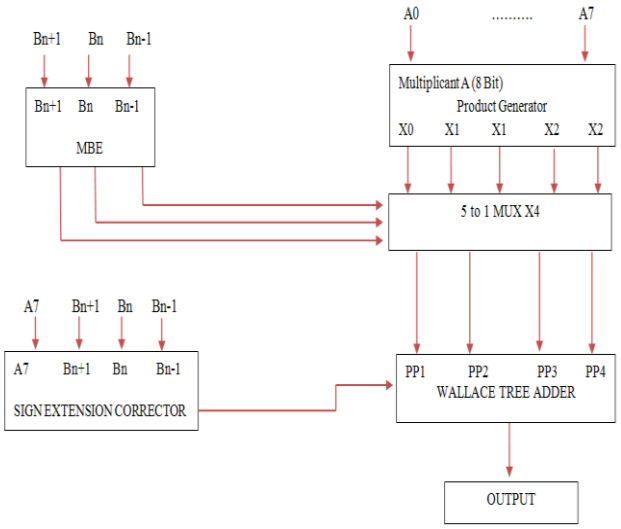

Fig. 3 Architecture of Booth Multiplier

Booth multiplier technique (Meier et al 1996) increases speed by reducing the number of partial products by half. An 8-bit booth multiplier needs only four partial products to be added instead of eight partial products generated using conventional multiplier. The architecture design for the modified Booths algorithm used in this design is shown in Figure 3 In order to achieve high-speed multiplication algorithms using parallel counters, the modified Booth algorithm has been proposed by Ki-seon Cho et al **[07],** and some multipliers based on the algorithms have been implemented for practical use. This type of multiplier operates much faster than an array multiplier for longer operands because its computation time is proportional to the logarithm of the word length of operands. The modified Booth multiplier on the processor is a major source of energy consumption for Digital Signal Processing programs. Given a pair of values to be multiplied, power should be reduced if the value is put together with the lower recoding weight into the second input of the modified Booth multiplier. The constant multiplication can be carried out by adding the partial product terms corresponding to the nonzero bit positions in the constant multiplier. To reduce the area and power consumption, the constant coefficient can be encoded such that it contains the fewest number of non zero bits. This can be accomplished using Canonic Signed Digit (CSD) representation discussed by Kim et al [5]. It compensates r the quantization error of CSD fixed-width multipliers in which the truncated bits are divided into major group and minor group. The effects of the truncated bits in the minor group are taken care of by a probabilistic estimation. Then, the desired error compensation bias is expressed in terms of the truncated bits in the major group. Finally, based on expression and error compensation bias circuit is designed using Karnaugh map method.

Low Power Full Adder Design

The design of full adders which forms the basic building blocks of all digital VLSI circuits has been undergoing considerable improvement, being motivated by three basic design goals, viz. minimizing the transistor count, minimizing the power consumption and increasing the speed, as postulated by Ahamed M. Shams et al [04].Pouya and Keivan Navi et al [08] emphasized an improvement in the performance of the Multiple Valued Logic OHRNS modulo rn Adder Circuit through transistor count minimization. XOR gates form the fundamental building blocks of full adders. Enhancing the performance of the XOR gates can significantly improve the performance of the adder (Navi et al [12]. A survey of literature reveals a wide spectrum of different types of XOR gates that have been realized over the years. The early designs of XOR were based on either eight transistors or six transistors that are conventionally used in most of the designs. All of the full adder circuits can be divided into two groups in point of output. The first group of full adders has full swing outputs (Zhuang and Wu [03]. The full adders of first group have good driving ability, high number of transistors, high area and usually higher power consumption in comparison to group two. The above logic approaches to design low power high performance full adders were suggested by Hosseinghadiry et al .[11]

Low-Power Full-Adder Based on CMOS Inverter

This full-adder is compression of inverters. Universal gates such as NOR, NAND and MAJORITY-NOT gates were implemented with a set of inverters by non-conventional approach. In the proposed design approach, the time consuming XOR gates are eliminated. As full-adders are frequently employed in a tree-structured configuration for high-performance arithmetic circuits, a cascaded simulation structure is employed to evaluate the full adders in a realistic and application environment. The circuits being studied were optimized for energy efficiency using 0.18m and 90 nm CMOS process technologies. The conventional adder is implemented with Transistors in CMOS technology. Conventional adder circuits do not function well below 1volt supply. The Complementary Pass-transistor Logic (CPL) adder, among the pass transistor logic styles, has the best performance and the lowest power delay product. The Transmission Function Full Adder (TFA), which is shown in Figure 4, uses 16 transistors is the opinion of Weste and Eshraghian.[01]

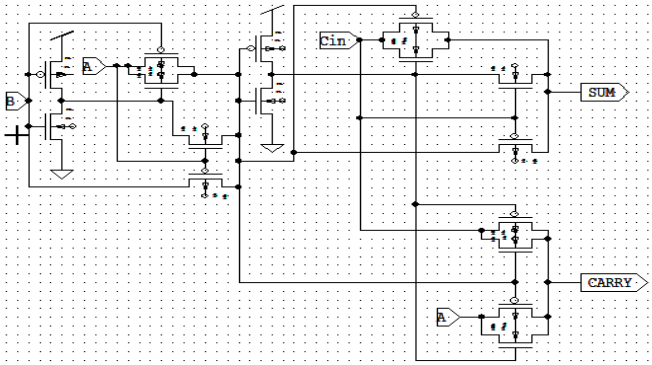

Fig. 4 CMOS standard 16 T Full Adder

Pull-up and pull-down logic is used to drive the load the same as the complementary pass logic the Transmission Gate full adder (TG). TG adder includes 20 transistors, and generates a + b and its complement to produce the sum and carry signals. It uses complementary input signals (a, b, c) as the complementary CMOS full adder, according to Vigneswaran, Mukundhan .[10]

Static Energy-Recovery Full Adder

As an initial step, Shalem et al [2] designed Static Energy Recovery Full adder (SERF) cell module. The cell uses only 10 transistors and it does not require inverted inputs. The design was inspired by the XNOR gate full adder design. In non-energy recovery design, the charge applied to the load capacitance during logic level high was drained to ground during the logic level low. It should be noted that the SERF adder has no direct path to the ground. The elimination of a path to the ground reduces power consumption, removing the Short Circuit Power (Psc) from the total power equation. The charge stored at the load capacitance is reapplied to the control gates. The combination in direct path to ground and the re-application of the load charge to the control gate makes the energy recovering full adder an energy efficient design. To the best of human knowledge, this new design has the lowest transistor count for the complete realization of a full adder.

V. CONCLUSION

In So far most of the works dealt with used to reduce the dynamic power consumption of the multipliers as well as full adder unit. The array multiplier is the worst case multiplier because it consumes highest amount of power. But the booth multiplier less power than the array multiplier. The Wallace Tree multiplier and Booth multiplier have nearly the same amount of delay while the Booth consumes less power than the other. In serial multiplier, the shift and add technique reduces the switching transition count in partial product unit but increases power consumption and delay. In low power full adder various transistor count full adder cells presented in this study are good but each type has different parametric values like power dissipation, area and delay. Hence, three new methods have been developed in this thesis work to reduce the power dissipation, area and delay of multipliers at the algorithm level of power abstraction. The fourth method presents both the theoretical and practical comparisons of all the adders which are taken into consideration. Consequently, an effective full adder cell is chosen to reduce the power consumption of the multiplier to the maximum level and it is seen that it also decreases the power delay product. It is evident that the Model-Sim and Xilinx are the vital tools in simulation and synthesis to evaluate the power consumption, area and delay of multipliers. Similarly Tanner is a vital tool for simulation and it can be used to evaluate the performance of the full adders and multipliers..

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