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An Implementation of BCD Converter for BCD Multipliers Using VHDL

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Abstract*—High speed, less usage of power consumption and area efficiency is some of the most valuable criterion for the fabrication of digits systems and high performance systems. Calculating the delay and area requirement of the multiplier is a major design issue. Though, area, speed and power are usually at variance parameter so that improving speed results mostly in larger areas. In present condition rate of increasing distinction of commercial, economic and network-based applications that process data in decimal arrangement. In our work, a new architecture decimal addition of Binary Coded Decimal (BCD) operands, which is the valuable design part of high speed low power multi-operand binary adders based on this add-3 digit or BCD adder, new architectures for higher order (n- digit) BCD adders such as ripple carry adder are developed. The proposed circuit designed is compared (both quality wise as well as quantity wise) with the existing circuits. Simulation results show that the proposed design of adder and multiplier based on add-3 digit BCD realizes an upgrading of delay shown to achieve faster than the obtainable ripple carry one. Since the scale of integration keeps growing day by day in the present times more difficult digital signal processing systems are being implemented on a very large scale integration chip. These signals giving out applications not only necessitate great calculation capacity but also consume substantial quantity of energy. Even as performance and design area remain to be the two important and valuable design tools, power utilization has turn into a critical concern in today "s VLSI system digital design.

***Keywords*— Wireless Sensor Network (WSN), Global Positioning System (GPS),Ssensor Nodes, Mobile Anchor Nodes And Broadcast, Etc …**

I. INTRODUCTION

High-performance energy-efficient arithmetic circuits with least area are essential for today's processors. In many arithmetic building blocks, designers are using conditional operations at the input stage, output stage, Some of them use XOR gates as input or output stages to control the signals as buffer or complement. In this kind of circuits, some of them use add by a constant value, some of them use an array of multiplexers as the output stage for the selection of different choices, and some of them use a combination In these circuits, the input signal is facing with conditional or unconditional complements in their path There is or (0100101)2. Binary to BCD converter module is critical because the number of binary-to-BCD conversion circuits needed for an n-digit fully parallel decimal multiplication is 2n, one circuit per partial product. On the other hand, the delay of the overall conversion art of multiplication hardware is the same as that of the delay f the single unit, since they all operate in parallel. In this aper, we proposed a new algorithm and architecture for 7-bit inary to BCD converter to cover 37 possible states equirements for BCD digit by digit multipliers. The proposed esign leads to a fast
nd energy efficient Binary to BCD converter with reasonable rea. The rest of this paper is organized as follows. Section II iscusses previous works in the field of decimal multiplication nd binary to BCD conversion. Section III describes the roblem formulation detail. Section IV presents the result arameters . Section V presents conclusion as well as future ork. and finally, references.

A. Objective

Addition requires a relatively small area and can meet the expense of fast operation. Multipliers are the key components of many high performance systems such as

microprocessors, digital signal processors and many countless applications

B. Motivation

A The center of any kind of digital processor and micro processor is its data path. Data path is one of the critical components which decide the key parameters of their design such as the clock frequency, area, power dissipation and look up table of the design. Adders and multipliers are the foremost components in the data path and they are of major anxiety for any digital designer of the data path [9]. The use of IP being popular for designing outsized systems, it is of more significance to consider the presentation of various digital adder and digital multiplier implementations that are offered with the commercially available IP. This thesis addresses on analyzing digital adders and that are available to be designed using VHDL.

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II. Literature Review

Farhana, et.al [2019] ,"A VLSI Implementation of Fast Binary to BCD Convertor using Complement Based logic design (CBLD)." This paper is proposed a new logic design for optimization of some arithmetic building blocks and design of multi-input multi-output combinational circuits. First, the efficiency of CBLD is proved with the optimization of some arithmetic blocks, then this technique is used for the design of the new architecture of Binary to BCD converter. By comparing the simulation results of the proposed CBLD designs with the conventional ones , we can say that the Proposed Architectural implementation of Shift-add by Constant has an improvement of 22%-138.7% on area and faster.[1] **Hossain, Nafiz ,et.al[2019], A Fast and Compact Binary to BCD Converter Circuit." BCD], BCD** (Binary Coded Decimal) representation is advantageous due to its finite place value representation, rounding, easy scaling by a factor of 10, simple alignment and conversion to character form. Hence, faster and efficient binary to BCD converter circuit is desired. In this paper, a compact binary to BCD converter circuit has been proposed. The proposed circuit can convert a 7-bit binary number to a 2-digit BCD number ranging from 0 to 99 which is the maximum possible value represented by 2-digit BCD number. Two conditional adder blocks are used to derive this output from input. An efficient algorithm has been proposed for the design of the converter circuit. Selection, partition and merging have been performed in the conversion process. The proposed circuit is 20.08% and 33.49% area and delay efficient, respectively than the existing best known converter circuits. Moreover, the proposed compact circuit can be utilized in vast and wide range applications wherever a conversion is required. The proposed compact converter circuit will subsequently influence the advancement in computation and manipulation of BCD digits in aspects of applications like scientific computation, embedded applications, digital communication and financial calculations. [2]. ***Das* Patil, Nikhil.et.al[2016] "Complimentary based logic design for arithmetic building blocks."** In this paper author presented New view of logic design with the name of Compliment Based Logic Design (CBLD) has been used to model the Various Arithmetic circuits in the field of VLSI. Comparison result obtained from Design vision of CBLD approach to their former counter parts shows that the CBLD version of BCD Adder/ subtract or consumes 60% less power and 19% less power than Modified reduced delay adder. Further, A new design approach is proposed in this paper to reduce the area and power of conventional structure for CSLAs architecture. This approach eliminates multiplexer and hence reduce number of gates required. This work offers the very [3]. ***Rangisetti, et. al. [2015], "Area-efficient and power-efficient binary to BCD converters*** In this paper author presented large reduction of area and also the total power. The compared results show that the modified CBEC-CSLA has a slightly larger delay, but the area and power of the 64-bit modified MRCA are significantly reduced by 51.5%, 77.1% 81% compared state of the art structures mentioned earlier. The modified RCA architecture is therefore, very less area occupying and very less power consuming. Texas Tech University [4]. **Juang, et.al.[2014], "Fast binary to BCD converters for decimal communications using new recoding circuits."** In this paper author presented By comparing these pre-layout simulation results of the proposed novel designs with the state-of-the-art , we can say that the Proposed Architectural implementation of Shift-add by Constant has an improvement of 22%-138.7% on area and 15.3%-226.2% on Power-Area product compared to existing best 4-3[2] algorithm and Fast Binary TO BCD algorithm, respectively. Range detection algorithm is 5.4%-52% more power-efficient than existing state of the art 4-3 algorithm and Fast Binary TO BCD algorithm. Moreover we demonstrated how we had an improvement on 3-3-1 in both area and delay in comparison with the previous circuit implementation [5]. **Mehta et.al,[2013] "High performance Vedic BCD multiplier and modified binary to BCD converter."**In this paper author In this paper we have proposed two different algorithms— one for binary to BCD conversion and another for NxN Vedic BCD multiplication and synthesized results of Vedic 2x2 BCD multiplier depicts it's efficiency in terms of slices and time of delay Now, this paper will boost the on-going research of the scholars in the field of decimal arithmetic. We can implement circuitry of decimal Division using *straight division methods*, multi-precision decimal square root using the *Dwandwa square-root algorithm*, decimal cube root using *Vedic cube root technique*; which are used simple multiplication and division. At last, Decimal Square and cube by using *Duplex property* and *Anurupya Sutra* of ancient Indian Vedic mathematics. These methods are mainly proposed only for the BCD number system; not for the binary systems. [6].

III.Proposed Algorithm

Decimal Arithmetic is widely utilized as a part of web based applications, commercial and budgetary purposes .Therefore the hardware that can support decimal arithmetic is turning into a need. The determination for the decimal balanced point algorithm were integrated which is a very slow process, complex and posses more area. These are executed using iterative methods or look up table based reduction technique. The inspiration behind BCD architecture enhancement is to expand their efficiency with expression of their speed and computational routine. In this thesis we have introduced an algorithm called shifting and adding by 3 algorithms that makes it area efficient over existing architecture of previous papers.

A. Algorithm (Shift and Add by constant) of-7bit

At Though the shifting and adding by 3 algorithms is not novel, the architecture execution by means of adding by constant which ultimately makes it area efficient is given away in figure 4.1.The most important objective of proposed algorithm is to perform proficient fixed bit binary coded decimal conversion

B. Iterative phase

In this phase, non-beacon nodes are localized iteratively. Node i with less than three Beacon nodes j uses sensor nodes which are already localized to obtain location coordinates. This is an iterative phase in which each non-beacon node wait for three beacon packet, as soon as it gets required number of the packet, computes their coordinate using multilateration. After that, node i broadcast their estimated coordinates which help to other neighbor nodes to compute their location coordinates. Repeat this process until all nodes gets their location which is well connected to the network; it means has more than three neighbors. The remaining nodes are localized in next phase

fig.1 Shift Add by Constant Architectural Implementation

This architecture is different as compared to other architecture. This structure can cover all 82 possible states (0 to 81) and do not need any extra hardware for its implementation which makes the circuit suitable and more dynamic for all applications. This architecture has two different modules. Figure 4.2 and 4.3 shows the following modules.

i. 3 -Bit Conditional Adder Blocks
ii.4 -Bit Conditional Adder Blocks.

Fig 2(A),Beacon Trajectory – Zig – Zag Diagonally

IV. SIMULATION RESULT

In this research paper In this work, Xilinx and Isim tools are used for timing analysis and synthesis. The simulation output for both 16-bit Binary to BCD adder is presented. After verifying the block diagram, the behavior of 16-bit Binary to BCD adder is checked by simulation process

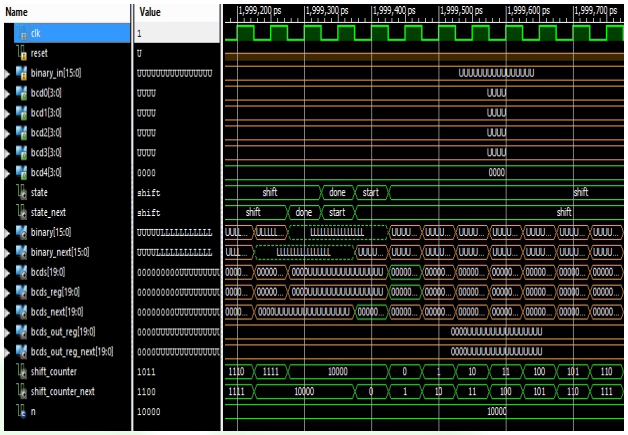
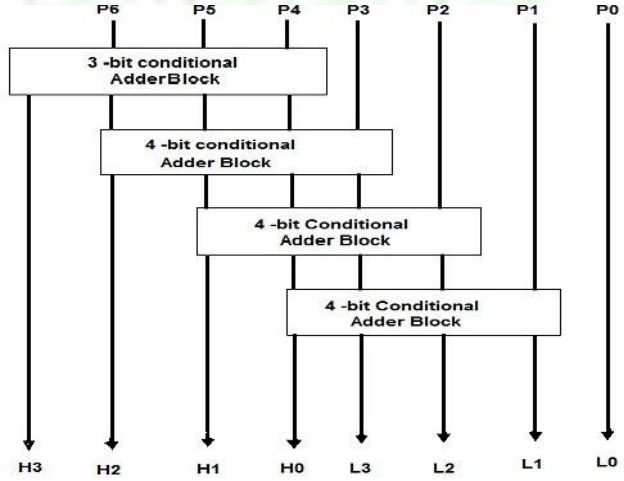


Fig.4.1 Simulation Waveform of Binary Coded Decimal Converter

In the simulation waveform of Binary Coded Decimal Converter in which state and state _next signal waveform of Binary Coded Decimal Converter shown. Which also shows reset on 0 and Binary Coded Decimal out register occupied output value and remaining length value represented by "L". And three process start, shift and done is mentioned which is a part of add-3 algorithm that used in our proposed circuit.



V. CONCLUSION

In this research paper A novel integrated Binary to Binary Coded Decimal multi-operand adder and converter

simultaneously and BCD multiplication algorithm has been proposed. The binary parallel multi-operand addition and conversion is performed by programmers for the conversion of Binary numbers to Decimal numbers. It is performed and calculated by shifting and adding that is by add-3 algorithm [1], and can be implemented using a smaller amount of number of gates in computer hardware, which ultimately makes it area efficient and BCD multiplier is design which shows new method for the reduction of the partial products in multiplication which is area efficient as compared to other designs. The proposed Binary Coded Decimal converter forms the center of the multi-operand Binary adder. Simulation results show the competence of our proposed BCD adder and multiplier in addition to multi operand decimal adder and multiplier with respect to exiting designs.

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