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An Implementation VLSI Architecture for FIR Filter using Multiple Vedic Multiplier and Kogge Stone Adder with Efficiency

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***Abstract*— Day by day numbers of the transistors are increasing at drastically manner. So designer must be kept in mind that device should be structured with less number of gates and other active and passive elements. Here we are designing a fast efficient Finite Impulse Response (FIR) filter using Vedic multiplier and Kogge Stone adder technique which can be used in digital signal processing, image signal processing, biological and mathematical solutions for transmitter and receiver part. Here we are using a Kogge Stone adder which is better than other parallel adder like Ripple carry, Look ahead carry and carry select adder. And multiplication calculations will be done by using Indian ancient Vedic mathematics technique. All the experiment and simulation will be done on Xilinx software, Spartan 3 series. The performance of implemented method including VLSI architecture is better as compared to the previous technique algorithm.**

Keywords*— *Vedic Multipliers; Kogge Stone Adder, VLSI Architecture, FIR Filter.

I. INTRODUCTION

The three most widely accepted metrics for measuring the performance of a circuit are power, delay and area. Minimizing area and delay has always been considered important, but reducing power consumption has been gaining prominence recently. With the increasing level of device integration and the growth in complexity of micro-elctronic circuits, reduction of power efficiency has come to fore as a primary design goal while power efficiency has always been desirable in electronic circuits. Recent advances in mobile computing and multimedia applications demand high performance and low-power VLSI digital signal processing (DSP) systems. One of the most widely used operations in DSP is finite-impulse response (FIR) filtering. In the existing method FIR filter is designed using array multiplier, which is having higher delay and power dissipation. The proposed method presents a programmable digital finite impulse response (FIR) filter for high performance applications. The FIR filter performs the weighted summations of input sequences and is widely used in video convolution functions, signal preconditioning, and various communication applications. Recently, due to the high-performance requirement and increasing complexity of DSP and multimedia communication applications, FIR filters with large filter taps are required to operate with high sampling rate, which makes the filtering operation very computationally intensive. Canonical-signed-digit and signed-power-of-two coefficient representations are widely used in the parallel implementation of FIR filters. Using those Techniques, the FIR filtering operation can be simplified to add and shift operations. Common sub expressions elimination and differential coefficients method also explore low-complexity design of FIR filters by minimizing the number of additions in filtering operations.

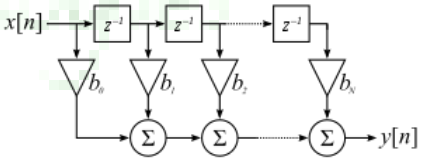

Figure 1 FIR Filter

II. LITERATURE REVIEW

Ashish Chouhan et al.(2019)- VLSI Architecture for 2×2 and 3×3 Fast Parallel FIR Filter using Vedic Multiplier and Kogge-stone Adder,2019, In the advanced digital technology the need is of high speed in real time system along with the improvement in implementation issue. Vedic Multipliers has been used to solve the typical and tedious engineering calculation by simple Vedic methods. Here in this paper we have proposed 2x2 and 3x3 parallel FIR filter with kogge stone adders replacing the traditional carry select adder The Vedic multiplier has also been

designed using this Kogge-stone adder to improve the propagation delay time and area on silicon chip. With this slight improve in the multiplier, great results have been achieved in signal processing tasks. All the design is implemented Xilinx software with different device family [1].

Deepak Kumar Patel et al. (2016), in this paper, the speed and area are now a day's one of the fundamental design issues in digital era. To increase speed, while doing the multiplication or addition operations, has always been a basic requirement of designing of advanced system and application. Carry Select Adder (CSA) is a fastest adder used in many processors to accomplish fast arithmetic function. Many different adder architecture designs have been developed to increase the efficiency of the adder. It is very commonly known that per second any processors performed millions of work functions in semiconductor industry. So when we do designing of multipliers, one of the main standards is performing speed that should be taken in the mind. In this paper, we propose a technique for designing of FIR filter using multiplier based on compressor and carry select adder. Performance of all adder designs is implemented for 16, 32 and 64 bit circuits. These structures are synthesized on Xilinx device family [2].

Basant Kumar Mohanty et al. (2016) - in this paper, transpose form finite-impulse response (FIR) filters are inherently pipelined and support multiple constant multiplications (MCM) technique that results in significant saving of computation. However, transpose form configuration does not directly support the block processing unlike direct form configuration. In this paper, we explore the possibility of realization of block FIR filter in transpose form configuration for area-delay efficient realization of large order FIR filters for both fixed and reconfigurable applications. Based on a detailed computational analysis of transpose form configuration of FIR filter, we have derived a flow graph for transpose form block FIR filter with optimized register complexity. A generalized block formulation is presented for transpose form FIR filter [3].

K. Durga et al. (2016) - in this paper, an effective engineering of FIR channel structure is exhibited. For accomplishing low power, reversible rationale method of operation is actualized in the plan. Territory overhead is the exchange off in the proposed outline. From the amalgamation comes about, the proposed low power FIR channel engineering offers 18.1 % of energy sparing when contrasted with the customary outline. The territory overhead is 2.6% for the proposed engineering [4].

Indranil Hatai et al. (2015) - this brief proposes a two-step optimization technique for designing a reconfigurable VLSI architecture of an interpolation filter for multistandard digital up converter (DUC) to reduce the power and area consumption. The proposed technique initially reduces the number of multiplications per input sample and additions per input sample by 83% in comparison with individual implementation of each standard's filter while designing a root-raised-cosine finite-impulse response filter for multistandard DUC for three different standards. In the next step, a 2-bit binary common subexpression (BCS)-based BCS elimination algorithm has been proposed to design an efficient constant multiplier, which is the basic element of any filter. This technique has succeeded in reducing the area and power usage by 41% and 38%, respectively, along with 36% improvement in operating frequency over a 3-bit BCS-based technique reported earlier, and can be considered more appropriate for designing the multi-standard DUC[5].

Thamizharasan .V et al (2012)- in An Efficient VLSI Architecture for FIR Filter using Computation Sharing Multiplier,"Volume 54– No.14, September 2012" Recent advances in mobile computing and multimedia applications demand high-performance and low-power VLSI digital signal processing (DSP) systems. One of the most widely used operations in DSP is finite-impulse response (FIR) filtering. In the existing method FIR filter is designed using array multiplier, which is having higher delay and power dissipation. The proposed method presents a programmable digital finite impulse response (FIR) filter for high-performance applications. The architecture is based on a computation sharing multiplier (CSHM) which specifically doing add and shift operation and also targets computation re-use in vector-scalar products. CSHM multiplier can be implemented by Carry Select Adder which is a high speed adder. A Carry-Select Adder (CSA) can be implemented by using single ripple carry adder and add-one circuits using the fast all-one finding circuit and low-delay multiplexers to reduce the area and accelerate the speed of CSA. An 4-tap programmable FIR filter was implemented in tanner EDA tool using CMOS 180nm technology based on the proposed CSHM technique. By adopting the proposed method for the design of FIR filter, the delay is reduced to about 43.2% in comparison with the existing method [6].

III. PROPOSED METHODOLOGY

3.1 Digital Fir Filter :-Digital signal processing algorithms are increasingly employed in modern wireless communications and multimedia consumer electronics, such as cellular telephones and digital cameras. The new generation of telecommunication equipment often requires the use of high order high-speed low-power Finite Impulse Response (FIR) filters. The output of an N tap FIR filter, which is the convolution of the latest L input samples, is given in equation (2). L is the number of coefficients h (k) of the filter, and x (n) represents the input time series.

$$Y[n] = \Sigma\, h[k]\, x[n-k] \qquad k= 0, 1, ..., N-1$$

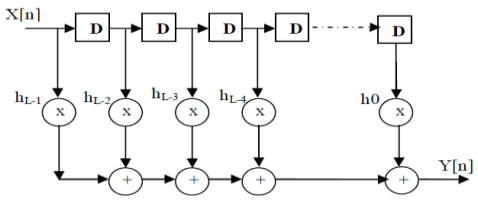

Figure 2 Traditional digital L-Tap FIR filter

In customary computerized FIR channels, augmentation operation with the channel coefficients h (k) and the

information x (n) are executed as the multipliers are required. Augmentation can be considered as a progression of rehashed increments. The number to be included is the multiplicand, the quantity of times that it is included is the multiplier and the outcome is the item. Hence adders, multipliers and defer components are critical segment to develop advanced FIR channel.

3.2 Introduction To Vedic Mathematics

Vedic mathematic is comprised with 16 sutras which were proposed by Jagadguru Swami Bharathikrishna Trithaji of Govardhan Peeth, Puri Jaganath (1884-1960). Urdhva Triyagbhayam sutra is applicable for all. Urdhva-Triyagbhayam sutra is essential technique for fast multiplication which is based on vertically and cross connections. This method is the part and parcial technique for low power VLSI design and Digital signal processing. Urdhav Triyagbhayam is a novel concept through which throughput is obtained parallel. Generation of partial products and their summation is obtained using this algorithm. The special feature is that differs from other conventional process is that it reduces the need of resources from process to operate at high frequencies requires.

IV. IMPLEMENTATION SOFTWARE

4.1 About the Software Tool

VHDL 14.1i Xilinx 14.1i is initial software for simulation result. Interfacing and work environment are different from other version. During the start the software click on new project and give the name according to file name and select the environment which in popup small screen as shows in Figure 3

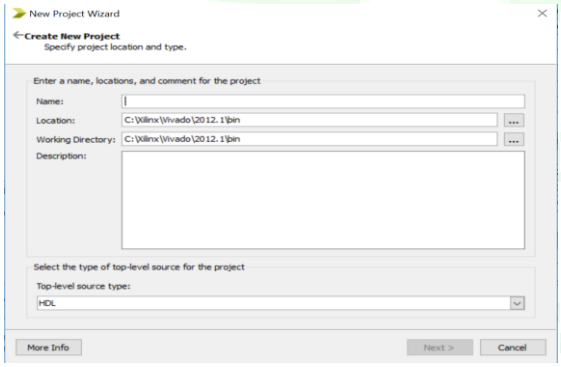

Figure3: Screenshot of 14.1i Software for Select New Project

V. IMPLEMENTATION ALGORITHM AND SIMULATION RESULT

5.1 Simulation Parameter

All the experiment analysis is done by 14.1i in Vertex device family. Xilinx 14.1i tool provides less propagation delay than to 6.2i Xilinx tool. The most important advantage of this tool is less memory with high speed analysis any complex logical circuit. Simulation and synthesize of finite impulse response (FIR) logical circuit can be enhanced by Xilinx design suit 14.1i Vertex device family series and device. Result analysis is always being done according to some important parameters like slice, IOBs, propagation delay, memory and LUTs.

5.1.1 Luts

LUT stands for look up table that reduces the complex mathematics calculations and provide the reduced processing time. Look up table uses so many complex applications such as signal processing, image processing, device modeling and other digital processing etc.

5.1.2 Slices

If the devices are connected in parallel form then it is called array of the devices. Generally look up table are comprised with number of slices. If the numbers of slices are increased then area will be increased. Numbers of slices are used less as possible as for better result and speed [16].

5.1.3 Propagation Delay

Generally, the ideal condition of the result is the output of the digital circuit should from level 0 to level 1 or level 1 to level 0 in zero time. But in practice, it takes finite time to switch output levels. The propagation delay of the device is basically the time interval between the application of an input pulse and the occurrence of the resulting output pulse. 53 The propagation delay is a very important characteristic of logic circuits because it limits the speed at which they can operate.

5.1.4 IOBs

Input output buffers are related to the fan in and fan out of the circuit. Number of gates is dependent on numbers of IOBs. So, for low propagation delay IOBs must be less [17].

5.2 Simulation Result

Figure 4 View Technology Schematic of 8-bit Kogge Sone Adder

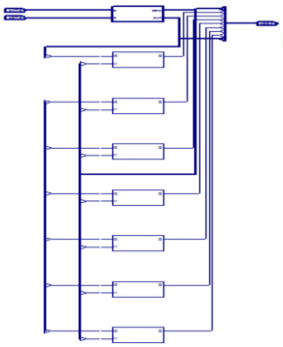

Figure 5 RTL View of 8-bit Kogge Sone Adder

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Device utilization summary:
---------------------------

Selected Device : 2vp2fg256-6

 Number of Slices:                        5  out of   1408     0%
 Number of 4 input LUTs:                  9  out of   2816     0%
 Number of bonded IOBs:                  25  out of    140    17%
Device utilization summary:
---------------------------

Selected Device : 2vp2fg256-6

 Number of Slices:                        5  out of   1408     0%
 Number of 4 input LUTs:                  9  out of   2816     0%
 Number of bonded IOBs:                  25  out of    140    17%
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Figure 6 Device Utilization summary of 8-bit Kogge Stone Adder

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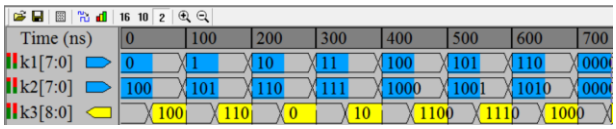

Figure 7 Output waveform of 8-bit Kogge Stone Adder

Clearly that the k1 and k2 is the input of the 8-bit Kogge Stone adder and k6 is the output of the kogge stone adder, in the figure 5.4 shows the output waveform of the 8-bit Kogge Stone adder.

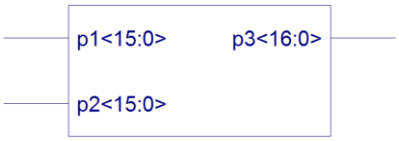

Figure 8 View Technology Schematic of 16-bit Kogge Sone Adder

```
Timing Summary:
---------------
Speed Grade: -6

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 5.699ns
Device utilization summary:
---------------------------

Selected Device : 2vp2fg256-6

 Number of Slices:                       10  out of   1408     0%
 Number of 4 input LUTs:                 17  out of   2816     0%
 Number of bonded IOBs:                  49  out of    140    35%
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Figure 9 Device Utilization summary of 16-bit Kogge Stone Adder

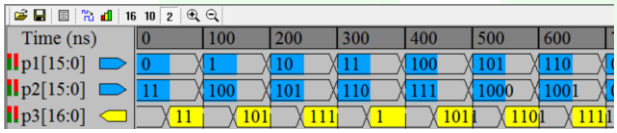

Figure 10 Output Waveform of 16-bit Kogge Stone Adder

We have implemented the proposed Vedic Multiplier using Kogge stone adder base on digital circuit. Basic architecture of Vedic multiplier Consists of full adder and half adder which requires less time to compute result. We have device summary of proposed multiplier and existing algorithm to achieve good computation speed compare to other shows in table 5.2. Show device utilization summary of 8-bit Vedic multiplier.

Table 1 Device utilization summary of Vedic Multiplier

Design	Width	Number of Slice	No. of 4-input LUTs	Gate Count	No. of IOBs	MCPD
8-bit Vedic Multiplier	8-bit	72	126	973	32	10.197 ns
16-bit Vedic Multiplier	16-bit	309	538	4405	64	12.038 ns
32-bit Vedic Multiplier	32-bit	1275	2218	18661	128	13.866 ns

Table 2 Comparison Result of Vedic Multiplier

Design	Width	Number of Slice	No. of 4-input LUTs	Gate Count	No. of IOBs	MCPD
VM using RCA [7]	8-bit	347	497	1111	34	23.18 ns
VM using KS Adder	8-bit	72	126	973	32	10.197 ns
VM using RCA [7]	16-bit	493	1243	5047	66	38.82 ns
VM using KS Adder	16-bit	309	538	4405	64	12.038 ns

Figure 9 shows the view technology schematic of 8-tap FIR filter using Vedic multiplier technique. In this figure 'fin' is the input of the 8-tap FIR filter using Vedic multiplier technique, 'h0, h1, h2, h3, h4, h5, h6, h7' is the input of the 8-tap FIR filter using Vedic multiplier technique and 'fout' is the input of the 8-tap FIR filter using Vedic multiplier technique.

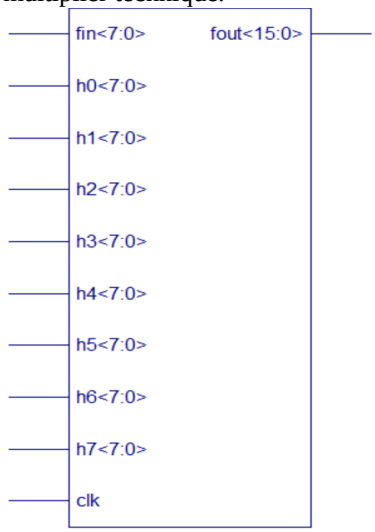

Figure 10: View Technology Schematic of FIR Filter using Vedic Multiplier

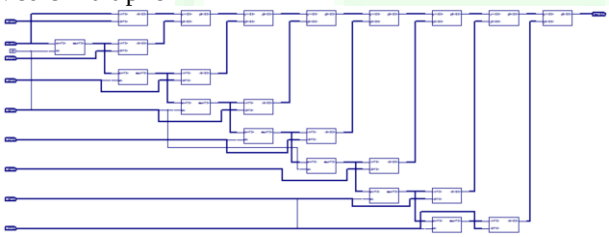

Figure 11: RTL View of FIR Filter using Vedic Multiplier

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Timing Summary:
---------------
Speed Grade: -6

   Minimum period: 1.459ns (Maximum Frequency: 685.401MHz)
   Minimum input arrival time before clock: 2.065ns
   Maximum output required time after clock: 24.186ns
   Maximum combinational path delay: 24.770ns
Device utilization summary:
---------------------------

Selected Device : 2vp2fg256-6

 Number of Slices:                      830  out of   1408    58%
 Number of Slice Flip Flops:             96  out of   2816     3%
 Number of 4 input LUTs:               1459  out of   2816    51%
 Number of bonded IOBs:                  88  out of    140    62%
 Number of GCLKs:                         1  out of     16     6%
```

Figure12: Device Utilization summary of FIR Filter using Vedic Multiplier

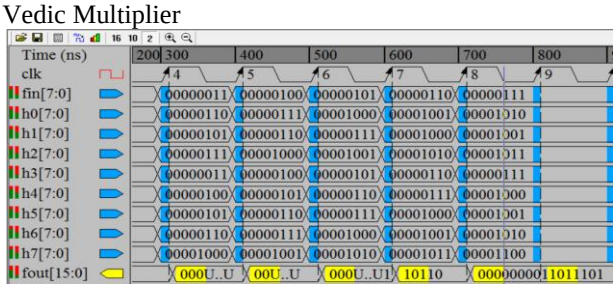

Figure 13: Output Waveform of FIR Filter using Vedic Multiplier

VI. CONCLUSION AND FUTURE SCOPE

5.1 Conclusion

This research work implemented the Vedic multiplier based digital FIR filter and compared its delay and memory usage of a traditional FIR filter designed using direct multiplier method, Braun multiplier method, Array and Baugh-Wooly multiplier method. The multiplier is an important signal processing technique which finds extensive application in many areas such as Image and speech processing, remote sensing, geophysics and communication engineering. The conventional methods used for convolution involve complexities and are not straight forward. The Vedic multiplier using Kogge Stone adder was designed using ISE tool in VHDL and it was found to work successfully with given inputs. From the synthesis report it was seen that the maximum combinational path delay is minimize.

5.2 Future Scope

FIR filters with proposed Vedic multiplier for the design and implementation of the different adder. As an extension to the present work, algorithms for composite radix could also be incorporated in the General radix algorithm to make it faster by reducing the operational complexity when the value of N is not a power of 2 or 4, but it can be expressed as a multiplication of various radices. In this thesis, two efficient designs of Adders are proposed which provides much optimized results in terms all important parameters considered. It would be interesting to implement higher bits modified Koggestone adder. This proposed architecture of Adders will be very efficient in various applications like Digital Electronics,

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