http://www.jctjournals.com

ISSN(ONLINE):2278 - 3814

Volume-12, Issue-07, July2023

JOURNAL OF COMPUTING TECHNOLOGIES (JCT)

International Journal

Page Number: 01-05

Efficient VLSI Architecture for FIR Filter using Multiple Vedic Multiplier and Kogge Stone Adder :A Review

[1]*Sonali Soni*, [2]*Prof. Amit Chauhan*

[1]*M.Tech Scholar*, [2]*Assistant Professor*,

[1,2] *Vidhyapeeth Institute of Science & Technology (VIST), Bhopal*

***Abstract*— With the advent of new technology in the fields of VLSI and communication, there is also an ever growing demand for high speed processing and low area design. It is also a well-known fact that the multiplier unit forms an integral part of processor design. Due to this regard, high speed multiplier architectures become the need of the day. In this thesis, it introduces a novel programmable multiplier architecture using high speed multiplication ancient Vedic math's techniques. A new high speed approach utilizing Vedic multiplier using Kogge Stone (KS) adder for addition has also been incorporated in the same and has been explored. Multiplication is an important function in arithmetic operations. A CPU (central processing unit) devotes a considerable amount of processing time in performing arithmetic operations. Multiplication requires substantially more hard-ware resources and processing time than addition and sub-traction. Digital signal processors (DSPs) are the technology that is omnipresent in engineering Discipline. Fast multiplication is very important in DSPs for digital filter, convolution, Fourier transforms etc.**

Keywords*— *Vedic Multipliers; Kogge Stone Adder, VLSI Architecture, FIR Filter.

I. INTRODUCTION

In signal processing the function of a filter is to remove unwanted parts of the signal, such as random noise, or to extract useful parts of the signal, such as the components lying within a certain frequency range.

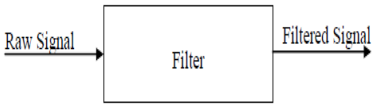

Figure 1.1: A Block Diagram of a Basic Filter

There are two types of filter analog and digital. FIR Filter is the kind of digital filter, which can be used to perform all kinds of filtering i.e. high pass, low pass, band pass and band reject etc.

1.1.1 Digital Filters :- A digital filter can be defined as a filter which operates on digital signals, such as sound represented inside a computer. In order to convert an output digital signal into analog form, it is necessary to perform additional signal processing to obtain the perfect result and is demonstrated. The process of converting an analog signal into digital form is performed by sampling with a finite sampling frequency. If an input signal contains frequency components higher than half the sampling frequency, it will cause distortion to the original spectrum [1].

1.2 Types Of Digital Filter

Filters can be classified in several different groups based on different criteria. The two major types of digital filters are:

1. Finite Impulse Response digital filters (FIR)
2. Infinite Impulse Response digital filters (IIR)

1.2.1 Finite Impulse Response

An FIR filter is also called as recursive filter in which in addition to input values it also uses previous output values. These, like the previous input values, are stored in the processor's memory. The word recursive literally means "running back", and refers to the fact that previously-calculated output values go back into the calculation of the latest output. The expression for a recursive filter therefore contains not only terms involving the input values (xn, xn-1, xn-2, ...) but also terms in yn1, yn-2, ...

1.2.2 Infinite Impulse Response digital filters (IIR)

Here, current output (yn) is calculated solely from the current and previous input values (xn, xn-1, xn-2 ...) this type of filter is also said to be non-recursive filters

1.3 Fir Filter Structure

A FIR filter is used to implement almost any type of digital frequency response. Usually these filters are designed with a multiplier, adders and a series of delays to create the output of the filter. The following figure shows the basic FIR filter diagram with N length. The result of delays operates on input samples. The values of hN-1 are the coefficients which are used for multiplication. So that the o/p at a time and that is the summation of all the delayed samples is multiplied by the appropriate coefficients.

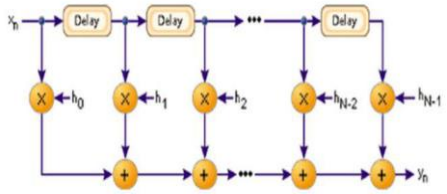

Figure 1 Logical Structure of FIR Filter

1.4 Algorithms For Multiplication

Algorithms that formalize the operation of multiplication generally consist of two steps: one that generates a partial product and the other that accumulates it with the previous partial products. The common multiplication method uses add and shift operators. The shift operation generates the partial products and the adder units sum them up. The general scheme for unsigned multiplication in base b is shown in Figure 1.2.

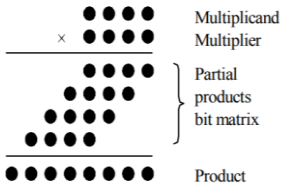

Figure 2 Multiplication Process

II. LITERATURE REVIEW

Deepak Kumar Patel et al. (2016), in this paper, the speed and area are now a day's one of the fundamental design issues in digital era. To increase speed, while doing the multiplication or addition operations, has always been a basic requirement of designing of advanced system and application. Carry Select Adder (CSA) is a fastest adder used in many processors to accomplish fast arithmetic function. Many different adder architecture designs have been developed to increase the efficiency of the adder. It is very commonly known that per second any processors performed millions of work functions in semiconductor industry. So when we do designing of multipliers, one of the main standards is performing speed that should be taken in the mind. In this paper, we propose a technique for designing of FIR filter using multiplier based on compressor and carry select adder. Performance of all adder designs is implemented for 16, 32 and 64 bit circuits. These structures are synthesized on Xilinx device family[1].

Basant Kumar Mohanty et al. (2016) - in this paper, transpose form finite-impulse response (FIR) filters are inherently pipelined and support multiple constant multiplications (MCM) technique that results in significant saving of computation. However, transpose form configuration does not directly support the block processing unlike direct form configuration. In this paper, we explore the possibility of realization of block FIR filter in transpose form configuration for area-delay efficient realization of large order FIR filters for both fixed and reconfigurable applications. Based on a detailed computational analysis of transpose form configuration of FIR filter, we have derived a flow graph for transpose form block FIR filter with optimized register complexity. A generalized block formulation is presented for transpose form FIR filter [2].

K. Durga et al. (2016) in this paper, an effective engineering of FIR channel structure is exhibited. For accomplishing low power, reversible rationale method of operation is actualized in the plan. Territory overhead is the exchange off in the proposed outline. From the amalgamation comes about, the proposed low power FIR channel engineering offers 18.1 % of energy sparing when contrasted with the customary outline. The territory overhead is 2.6% for the proposed engineering [3].

Indranil Hatai et al. (2015), this brief proposes a two-step optimization technique for designing a reconfigurable VLSI architecture of an interpolation filter for multistandard digital up converter (DUC) to reduce the power and area consumption. The proposed technique initially reduces the number of multiplications per input sample and additions per input sample by 83% in comparison with individual implementation of each standard's filter while designing a root-raised-cosine finite-impulse response filter for multistandard DUC for three different standards. In the next step, a 2-bit binary common subexpression (BCS)-based BCS elimination algorithm has been proposed to design an efficient constant multiplier, which is the basic element of any filter. This technique has succeeded in reducing the area and power usage by 41% and 38%, respectively, along with 36% improvement in operating frequency over a 3-bit BCS-based technique reported earlier, and can be considered more appropriate for designing the multi-standard DUC [4].

S. Padmapriya et al. (2015), linear phase FIR filter banks form an integral part of the ISO/IEC JPEG 2000 image coding standard. One feature they enable is lossless sub band coding based on reversible filter bank implementations. While this meshes well with symmetric boundary-handling techniques for whole-sample symmetric (odd- length) linear phase filters, there are obstructions with half- sample symmetric (even-length) filters, a fact that influenced the JPEG 2000 standard. We show how these obstructions can be overcome for a class of half-sample symmetric filter banks by employing lattice vector quantization to ensure symmetry- preserving rounding in reversible implementations [5].

Kiran Joy et al. (2014) Man has achieved wonders in his race from the stone age to the supersonic age. These wonders can be understood from the modern technologies. Technological advancements are becoming a part and parcel of this world. More and more technologies with lot of features and advantages are arising. Reversible logic is one such emerging concept. One of the main characteristics of reversible circuits is their less power consumption. As the technology improves, the number of components and

hence the number of transistors packed on to the chip also increases. This causes increase in power consumption. Hence reduced power consumption argued by the reversible logic concept has adequate importance in the present scenario. Reversible logic has a wide application in low power VLSI circuits. This paper aims at promoting the concept of reversible logic by implementing a model of a FIR filter using the reversible Fredkin gate [6].

Ravi H Bailmare et al. (2014) presented a low power and high speed FIR filter designs by using first order difference between inputs and various orders of differences between coefficients. Further, they adopted the Distributed Arithmetic (DA) architecture to exploit the probability distribution aiming to reduce the power consumption. The design was applied to an example FIR filter to quantify the energy savings and speedup. It showed lower power consumption than the previous design with the comparable performance [7].

M. Usha et al. (2014) developed a custom Very-Large-Scale Integration architecture, which consists of a reconfigurable hardware substrate and a hybrid-genetic algorithm responsible for resolving the optimal configuration for the reconfigurable components of the substrate. The reconfigurable hardware was specifically tailored for the implementation of multiplier-less symmetrical FIR filters based on the primitive operator technique, while the architecture of the hybrid genetic algorithm aims to improve the quality of the realized filters and speeding up the time required for their realization. Power analysis demonstrates that the filters, which are implemented by their architecture, consumed considerably less power than industrial Field Programmable Gate Arrays, targeting similar applications [8].

III. PROPOSED METHODOLOGY

3.1 Digital Fir Filter

Digital signal processing algorithms are increasingly employed in modern wireless communications and multimedia consumer electronics, such as cellular telephones and digital cameras. The new generation of telecommunication equipment often requires the use of high order high-speed low-power Finite Impulse Response (FIR) filters. The output of an N tap FIR filter, which is the convolution of the latest L input samples, is given in equation (3.1). L is the number of coefficients h (k) of the filter, and x (n) represents the input time series.

$$Y[n] = \Sigma\, h[k]\, x[n-k] \qquad k= 0, 1, ..., N-1$$

The conventional L tapped delay line realization of this inner product is shown in Figure 3.1. This implementation translates to L multiplications and L-1 additions per sample to compute the result. This can be implemented using a single Multiply Accumulate (MAC) engine, but it would require L –MAC cycles, before the next input sample can be processed.

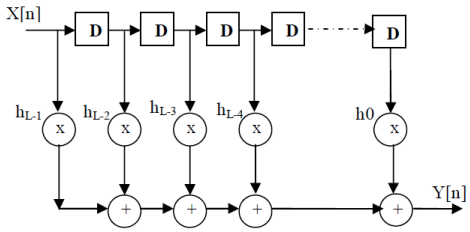

Figure 3 Traditional digital L-Tap FIR filter

In customary computerized FIR channels, augmentation operation with the channel coefficients h (k) and the information x (n) are executed as the multipliers are required.

Augmentation can be considered as a progression of rehashed increments. The number to be included is the multiplicand, the quantity of times that it is included is the multiplier and the outcome is the item. Hence adders, multipliers and defer components are critical segment to develop advanced FIR channel. A definitive point of this examination is to outline a rapid and low power computerized FIR channels. In this exploration work, FIR channel is planned with cluster multiplier which thusly framed with eight unique sorts of snake units. So also, FIR channel is outlined with Braun, limb wooly and Wallace tree multiplier which thusly are framed with eight unique sorts of viper units. Among the outline of computerized FIR channel with four unique sorts of multiplier structures in which each structures is planned with an alternate kind of snake unit, Wallace tree multiplier structure creates better outcome in edge misfortune issue, speed and influence.

3.2 Introduction To Vedic Mathematics

Vedic mathematic is comprised with 16 sutras which were proposed by Jagadguru Swami Bharathikrishna Trithaji of Govardhan Peeth, Puri Jaganath (1884-1960). Urdhva Triyagbhayam sutra is applicable for all. Urdhva-Triyagbhayam sutra is essential technique for fast multiplication which is based on vertically and cross connections. This method is the part and parcial technique for low power VLSI design and Digital signal processing. Urdhav Triyagbhayam is a novel concept through which throughput is obtained parallel. Generation of partial products and their summation is obtained using this algorithm. The special feature is that differs from other conventional process is that it reduces the need of resources from process to operate at high frequencies requires.

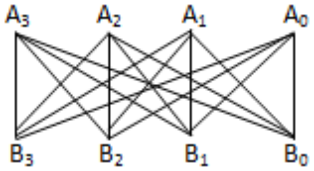

Figure 4 A 4 bit Vedic Multiplication

Block diagram of 4-bit Vedic multiplier is shown in figure 3.4. Here (*A*3,*A*2,*A*1,*A*0) and (*B*3,*B*2,*B*1,*B*0) bits are multiplied together and produce 8 bit output sequence. So, Vedic mathematic provides the less complexity then to other.

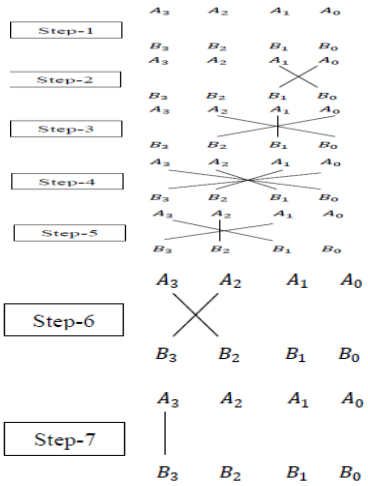

Figure 5 Steps of Vedic Multiplication for the 4-bit Information

A step of Vedic Multiplication for the 4-bit Information is shown in figure 3.3. The proposed Vedic multiplier is based on the Vedic multiplication formulae (Sutras). These Sutras have been customarily utilized for the duplication of two numbers in the decimal number framework. In this work, we apply the same thoughts to the paired number framework to make the proposed calculation perfect with the computerized equipment.

We explore a novel method to further enhance the speed of a Vedic mathematics multiplier by replacing the existing full adders and half adders of the Vedic mathematics based multipliers with compressors by using Urdhva-triyakbhyam sutra.

IV. IMPLEMENTATION SOFTWARE

4.1 About the Software Tool

Condition setup is the workplace or apparatuses on which result examination has been done in Xilinx 14.1i. Xilinx is the exceptionally solid programming apparatus to investigation and reproduce the mind boggling circuits. There are such a large number of variants for Xilinx programming, for example, 6.1i, 9.1i, 10.2i, 13.1i and 14.2i. For the most part two programming dialect are utilizing VHDL and Verilog. VHDL is an acronym for VHSIC equipment depiction dialect (VHSIC is an acronym for fast incorporated circuits). It is an equipment depiction dialect that can be utilized to demonstrate a computerized framework at many levels of retention running from the calculation level to the door level [14]. VHDL permits clients or software engineers to utilize certain squares which contain certain arrangement of consecutive articulations. One such square is known as a procedure. The (<=) administrator, it is known as the task administrator and is utilized just to assign qualities to signals. For factors the administrator utilized is (:=)

V. CONCLUSION AND FUTURE SCOPE

5.1 Conclusion

This research work implemented the Vedic multiplier based digital FIR filter and compared its delay and memory usage of a traditional FIR filter designed using direct multiplier method, Braun multiplier method, Array and Baugh-Wooly multiplier method. The multiplier is an important signal processing technique which finds extensive application in many areas such as Image and speech processing, remote sensing, geophysics and communication engineering. The conventional methods used for convolution involve complexities and are not straight forward. The Vedic multiplier using Kogge Stone adder was designed using ISE tool in VHDL and it was found to work successfully with given inputs. From the synthesis report it was seen that the maximum combinational path delay is minimize. Eventually, in this thesis we have structured a fast FIR filter circuit which is based on Vedic multiplier and Kogge stone adder. In the previous research work FIR filter has been designed only by the RCA, CSA, HA, and FA but not efficient. But in this thesis work we have designed fast FIR filter technique based on Vedic multiplier and Kogge Stone adder.

5.2 Future Scope

FIR filters with proposed Vedic multiplier for the design and implementation of the different adder. As an extension to the present work, algorithms for composite radix could also be incorporated in the General radix algorithm to make it faster by reducing the operational complexity when the value of N is not a power of 2 or 4, but it can be expressed as a multiplication of various radices. In this thesis, two efficient designs of Adders are proposed which provides much optimized results in terms all important parameters considered. It would be interesting to implement higher bits modified Koggestone adder. This proposed architecture of Adders will be very efficient in various applications like Digital Electronics, Signal Processing and Robotics as Floating Point Arithmetic. Designed high speed convolution technique can use for designing the filter to filter the blurred signal. This can be used for image processing and digital signal processing technique. By using high speed multiplier ALU, GPU and CPU can be designed. The algorithms presented may be extended to multidimensional data.

References

[1] Thamizharasan .V Et all "An Efficient VLSI Architecture for FIR Filter using Computation Sharing Multiplier on International Journal of Computer Applications (0975 – 8887) Volume 54– No.14, September 2012.

[1] Deepak Kumar Patel, Raksha Chouksey and Dr. Minal Saxena, "Design of Fast FIR Filter Using Compressor and Carry Select Adder", 2016 3rd International Conference on Signal Processing and Integrated Networks (SPIN).

[2] Basant Kumar Mohanty, and Pramod Kumar Meher, "High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 78, No.06, April 2016.

[3] K. Durga and Mrs. A. Sivagam, "Efficient Adaptive RLFIR Filter based on Distributed Arithmetic Logic Using Reversible gates", International Conference on IEEE 2016.

[4] Indranil Hatai, Indrajit Chakrabarti, and Swapna Banerjee, "An Efficient VLSI Architecture of a

Reconfigurable Pulse-Shaping FIR Interpolation Filter for Multi-standard DUC", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 23, No. 6, June 2015.
[5] S. Padmapriya and Lakshmi Prabha V., "Design of a power optimal reversible FIR filter for speech signal processing", International Conference, pp. 01-06, ICCCI 2015.
[6] Kiran Joy and Binu K Mathew, "Implementation of a FIR Filter Model using Reversible Fredkin Gate", Control, Instrumentation, Communication and Computational Technologies (ICCICCT), 2014 International Conference on IEEE Xplore**,** 22 December 2014.
[7] Ravi H Bailmare, S. J. Honale And Pravin V Kinge, "Design And Implementation of Adaptive FIR Filter using Systolic Architecture", In International Journal of Current Engineering And Technology , Vol.4, No.3, June 2014.
[8] M. Usha, R. Ramadoss, "An Efficient Adaptive Fir Filter Based On Distributed Arithmetic", International Journal of Engineering Science Invention, Vol. 3, Issue. 4, pp. 15-20, April 2014.
[9] Sang Yoon Park and Pramod Kumar Meher, "Low power, High-throughput And Low- Area Adaptive FIR Filter Based on Distributed Arithmetic", in IEEE Transactions On Circuits And Systems-ii, Vol. 60, No. 6, pp. 346- 350, 2013.
[10] Basant K. Mohanty, And Pramod Kumar Meher, "A High-Performance Energyefficient Architecture For FIR Adaptive Filter Based On New Distributed Arithmetic Formulation Of Block LMS Algorithm", In IEEE Transactions On Signal Processing, Vol. 61, No. 4, February, 2013.
[11] Pallavi Saxena, Urvashi Purohit, Priyanka Joshi, "Analysis of Low Power, Area Efficient and High Speed Fast Adder", In International Journal Of Advanced Research In Computer And Communication Engineering, Vol. 2, Issue 9, September 2013.
[12] H. Thapliyal, N. Ran-Ganathan and S. Kotiyal, "Design of Testable Reversible Sequential Circuits", IEEE Transactions on VLSI, pp. 1-9, 2012.
[13] M. Chuang and C. Wang, "Reversible sequential element designs", Proceedings of the IEEE Asia and South Pacific Design Automation Conference, pp. 420-425, 2007.
[14] G. Challa Ram and D.Sudha Rani, "Area Efficient Modified Vedic Multiplier", 2016 International Conference on Circuit, Power and Computing Technologies (ICCPCT).

