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Designing and Simulation of Multiple Complex Gate with 70nm Technology in Microwind with Efficient Energy and Memory Saving: - A Review

[1]Yashasvi, [2]Arpan Dwivedi

[1]M.tech Student, [2]Professor and Dean

[1,2] SAM College of Engineering & Technology

Abstract— Digital system implemented by using conventional gates like Designing and Simulation of Multiple Complex Gate with 70mn Technology in Microwind with Efficient Energy and Memory Saving gates dissipates a major amount of energy in the form of bits which gets erased during logical operations. This problem of energy loss can be solving by using reversible logic circuits in place of conventional circuits. This problem of energy loss can be solving by using reversible logic circuits in place of conventional circuits. Reversible logic is widely being considered as the potential logic design style for implementation in modern nanotechnology and quantum computing. Reversibility has become the most promising technology in digital circuits designing. Reversible logic may be a promising computing design paradigm that presents a technique for constructing computers that produce no heat dissipation. Reversible computing emerged as results of the applying of quantum physics principles towards the event of a universal computing device.

Keywords— Microwind, Complex Gate, Energy, Logic Gate, Dissipation and Memory.

I. INTRODUCTION

Reversible rationale is a rationale configuration style in which there is a balanced mapping between the info and the yield vectors. If a framework is irreversible then eradicating a bit causes kTln2 joules of warmth vitality where k is the Boltzmann's steady and T is the outright temperature of the earth. This kTln2 joule of warmth vitality won't be scattered if a calculation is performed reversibly in light of reversible rationale circuits. Reversible rationale has broad applications in developing innovations, for example, quantum registering, quantum speck cell automata, optical processing, and so on. The real utilization of reversible rationale lies in quantum registering. A quantum PC will be seen as a quantum arrange (or a group of quantum systems) made out of quantum rationale entryways; each door playing out a rudimentary unitary operation on one, two or more two-state quantum frameworks called qubits. Quantum systems must be worked from reversible legitimate parts [1]. A Sixteen piece viper can include 16 bits in a solitary cycle and henceforth frames the indispensable segment of many figuring frameworks including broadly useful processor and advanced flag processors and some more.

Landauer demonstrated that parallel rationale circuits manufactured utilizing conventional irreversible entryways unavoidably prompt vitality dispersal, paying little mind to the innovation used to understand the doors. Zhirnov demonstrated that power dispersal in any future CMOS will prompt an incomprehensible warmth evacuation issue and in this manner the accelerating of CMOS gadgets will be inconceivable eventually which will be come to before 2020. Bennett turned out to be disseminated in a parallel rationale circuit, it is vital that the circuit be worked from the reversible entryways. A door (or circuit) is reversible on the off chance that it is a balanced mapping between sets of info and yield values. In this way all yield vectors are only stages of info vectors. (Such a circuit can be depicted by a twofold stage framework. Bennett's hypothesis proposes that each future (double) innovation should utilize some sort of reversible doors so as to diminish control scattering. This is likewise valid for different esteemed reversible rationales, which is an extra favorable position on the grounds that the multi-valued ness without anyone else's input shows a few potential points of interest over double rationale. These possibilities of MV rationale so far have not been exploited since they convey no innovative changes when connected to existing advances, for example, CMOS. All these major consequences of Landauer, Bennett and Zhirnov areinnovation free yet for all intents and purposes material to future nanotechnologies, particularly to quantum innovation just like the most progressive of all the nano-

advancements. They are additionally pertinent in quantum spots and DNA circuit acknowledgment advances. The input and output vector of an N-input and N-output reversible logic gate or N X N reversible logic gate.

II. LITERATURE SURVEY

Mohamadreza Eslami, et.al 2021 Design and Simulation of Optical XNOR Logic Gate Based on MEMS Technology, Prototypes of computers, or processors, were based almost exclusively on mechanical devices. Although electronic processors have become increasingly dominant over the past few decades, Recent advances in the technology of manufacturing 3D electromechanical components in micro and nano sizes have created new techniques for building complex microstructures that are of interest to researchers in new research In the field of mechanical computing. In this paper, we present a new XNOR logic gate design approach that can be built based on micro-electromechanical logic gates. One of the main advantages of this method is the ability to combine multi-physical as well as compatibility with the CMOS manufacturing process, as well as lower power consumption compared to logic gates consisting of several CMOS transistors. In this design, we have designed and simulated an XNOR logic gate using the multi-physics capability of Comsolsoftware and as well as using optical, electronic, mechanical and electro-static physics, whose inputs will be both electrical and optical signals. In this paper, according to the above selected design, by modeling and simulating different input modes of this logic gate, we examine the effect of each mode on the output of the gate as well as other features such as structure life, power consumption and resonant frequency. The proposed gate structure has a resonant frequency of 46 kHz and is highly reliable because it can operate without mechanical connection of the MEMS operator to logic inputs **[01].**

Tie Mei et. al. 2021, A mechanical metamaterial with reprogrammable logical functions, Embedding mechanical logic into soft robotics, microelectromechanical systems (MEMS), and robotic materials can greatly improve their functional capacity. However, such logical functions are usually pre-programmed and can hardly be altered during in-life service, limiting their applications under varying working conditions. Here, we propose a reprogrammable technological metamaterial (ReMM). Logical computing is achieved by imposing sequential excitations. The system can be initialized and reprogrammed via selectively imposing and releasing the excitations. Realization of universal combinatorial logic and sequential logic (memory) is demonstrated experimentally and numerically. The fabrication scalability of the system is also discussed. We expect the ReMM can serve as a platform for constructing reusable and multifunctional mechanical systems with strong computation and information processing capability **[05].**

Yuanping Song,et al 2019, Additively manufacturable micro-mechanical logic gates, Early examples of computers were almost exclusively based on mechanical devices. Although electronic computers became dominant in the past 60 years, recent advancements in three-dimensional micro-additive manufacturing technology provide new fabrication techniques for complex microstructures which have rekindled research interest in mechanical computations. Here we propose a new digital mechanical computation approach based on additively manufacturable micro-mechanical logic gates. The proposed mechanical logic gates (i.e., NOT, AND, OR, NAND, and NOR gates) utilize multi-stable micro-flexures that buckle to perform Boolean computations based purely on mechanical forces and displacements with no electronic components. A key benefit of the proposed approach is that such systems can be additively fabricated as embedded parts of micro architected met materials that are capable of interacting mechanically with their surrounding environment while processing and storing digital data internally without requiring electric power **[02].**

Sally Ahmed et al 2019, A Compact Adder and Reprogrammable Logic Gate Using Micro-Electromechanical Resonators With Partial Electrodes, The design principles and experimental demonstration of a compact full adder along with a reprogrammable 4-input logic gate are presented. The proposed solution for implementation of digital circuits is based on a clamped– clamped micro-beam resonator with multiple splitelectrodes, in which the logic inputs tune the resonance frequency of the beam. This technique enables re-programmability during operation, and reduces the complexity of the digital logic design significantly; as an example, for a 64-bit adder, only 128 micro resonators are required, compared to more than 1500 transistors for standard complementary metal–oxide–semiconductor (CMOS) architectures. We also show that an optimized simulated micro-resonator-based full adder is 45 times smaller than a CMOS mirror adder in 65-nm technology. While the energy consumption of this early generation of micro-resonator logic gates is higher than the CMOS solutions, we show that by careful device optimization and shrinking of the dimensions, femtojoules energy consumption and MHz operation, required by Internet of Things applications, are attainable **[04].**

Saad Ilyas et. al. ,2017, Multi-function and cascadable mems logic device, We present a reprogrammable Microelectromechanical systems (MEMS) logic device that can perform the fundamental logic gate AND, a universal logic gate NAND, and a tristate logic gate using mixed-frequency excitation. The concept is based on exciting combination resonances due to the mixing of two or more input signals. The device vibrates at two steady states; a high state when the combination resonance is activated and a low state when no resonance is activated. These vibration states are assigned to logical value 1 or 0 to realize these logic gates. Using AC signals to drive the resonator and to execute the logic inputs unifies the input and output wave forms of the logic device, thereby opening the possibility for cascading among logic devices. Moreover, the ability to perform these logic operations at any input frequency using frequency mixing techniques allows for overcoming the limitation of having a fixed operating frequency. These characteristics of such logic devices lay down the basis to achieve complex computing operations **[03].**

Gopi Chand Naguboina et.al. 2017 "Design and

Synthesis of Combinational Circuits Using Reversible Decoder in Xilinx", reversible rationale is the rising field for inquire about in exhibit period. The point of this paper is to acknowledge diverse kinds of combinational circuits like full-viper, full- subtractor, multiplexer and comparator utilizing reversible decoder circuit with least quantum cost. Reversible decoder is composed utilizing Fredkin doors with least Quantum cost. There are numerous reversible rationale doors like Fredkin Gate, Feynman Gate, Double Feynman Gate, Peres Gate, Seynman Gate and some more. Reversible rationale is characterized as the rationale in which the number yield lines are equivalent to the quantity of info lines i.e., the n-information and k-yield Boolean capacity F(X1, X2, X3,… ,Xn) (alluded to as (n, k) work) is said to be reversible if and just in the event that (I) n is equivalent to k and (ii) each info design is mapped extraordinarily to yield design [06].

Marcin Bryk et.al. 2016, **"Encryption using reconfigurable reversible logic gate and its simulation in FPGAs"**, recently an approach to encryption/decryption based on using reversible logic circuits has been proposed. The reason for this is that conventional microelectronic technologies are reaching their limits. On the other hand, reversible logic circuits can decrease energy dissipation theoretically to zero. This paper presents a solution to designing encryption schemes based entirely on reversible logic. In our solution a building block of an encryption scheme is a cascade of 4-input reversible gates. In this way the building block can perform any reversible 4-variable function. For this purpose a reconfigurable reversible gate has been proposed. The design ofsuch a reconfigurable gate built from standard reversible gates, i.e. NOT, CNOT, Toffoli and Fredkin gates, is presented. In the paper a complete scheme for encryption/decryption of 8-bit data is described using VHDL language and its quantum cost is calculated. Simulation and verification of this scheme in FPGAs conclude the paper **[07].**

Lafifa Jamal et.al. 2015, "Design and Implementation of a Reversible Central Processing Unit", Quantum computing necessitates the design of circuits via reversible logic gates. Efficient reversible circuit can be constructed by achieving low ancilla count, reducing logical depth and lowering Quantum costs. Generalized Peres gates have recently been realized with very low Quantum Cost (QC) by utilizing Quantum rotation gates. This is utilized in recent literature for efficient reversible circuit constructions for symmetric Boolean functions. In this paper, we extend this line of construction further by demonstrating efficient realization of adder circuits. In particular, we revisit the adder construction of Vedral, Barenco and Eckert to show that improvement of gate count and QC is achievable by exploiting a construction based only on Peres gates **[08].**

Junchao Wang et.al. **2014, "A Carry look ahead adder designed by reversible logic"** , this paper says that a lot of attentions have been attracted by the reversible logic due to the characteristic of zero energy dissipation. Reversible logic can be applied in fields such as low power CMOS circuits, quantum computation and DNA computing. In this paper, the author proposed a 16 bit carry look-ahead adder is constructed by four 4 digits groups based on the theory of reversible logic, which has the advantages of theoretical zero power dissipation and high efficiency **[09].**

James Donald et.al. 2008 "Reversible logic synthesis with fredkin and peres gates" in this paper it has been realized that quantum computing is one of the latest technologies using reversible logic. It is observed that increasing growth of transistor density, power consumption will reach their limits in conventional technologies. In conventional Circuits during the logic operations bits of information is erased resulting dissipation of energy in significant amount. Thus, if Circuits are designed so that information bits can be preserved, the power use can be reduced. In case of reversible logic computation, the information bits are not lost. We can use reversible logic technology for minimizing the power consumption, heat dissipation, increasing speed etc. This paper describes various logic gates based on reversible logic like Toffoli, Peres, Fredkin, and Feynman etc. A comparative between classical and quantum logic gates is also given on various parameters along with limitations of conventional computing **[10].**

III. PROBLEM STATEMENT

As seen from the literature survey the importance of Complex logic in digital system design the approximation zero power is lost in reversible logic, and by studying different reversible logic gate it is found that peres gate has the lowest number of quantum cost so in this thesis implementation of Complex Logic Gate has been implemented using simple multiple Gate.

IV. CONCLUSION

As we realize that the rudiments of reversible figuring depend on the relationship between entropy, heat move between atoms in a framework, the likelihood of a quantum molecule possessing a specific state at any given time, and the quantum electrodynamics between electrons when they are in close nearness. The essential guideline of reversible registering is that a injective gadget with an indistinguishable number of information and yield lines will produce a computing environment where the electrodynamics of the system allow for calculation of all future states based on known past states, and the system reaches every possible state, resulting in no heat dissipation. Hence in this design we have proposed a design to calculate the power that is analogous to heat dissipation and to compare the delay and increase the number of logical arithmetic operation. The numbers of steps followed in this thesis are as under:

1. 1.Two highly programmable, low-cost and low-delay 4*4 reversible logic gates were presented, verified and compared to similar logic structures already published.
2. 2.The proposed modified fredkin gate as the best existing 4×4 reversible gates in terms of cost, delay and logical output calculations.
3. 3.The gates were then implemented in reversible arithmetic logic units. These new decoder, multiplier designs are advantageous to previously published work in implementations that favor low delay and high logical calculation output, which is desirable for realization of a reversible central processing unit.

4. 4.The proposed designs are then integrated in the design of a novel reversible combinational circuit.

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