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Implementation of Multiple Complex Gate with 70nm Technology in Microwind with Energy Efficient Model

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Abstract— The complex Circuit has the promising applications in rising registering worldview for example, quantum figuring, quantum speck cell automata, optical registering, and so forth. In reversible rationale doors there is a novel coordinated mapping between the information sources and yields. To produce a helpful door work the reversible entryways require some consistent subordinate sources of info called ancilla inputs. Likewise to keep up the reversibility of the circuits some extra unused yields are required that are alluded as the waste yields. The quantity of ancilla sources of info, number of rubbish yields and quantum cost assumes a vital part in the assessment of reversible circuits. In this way limiting these parameters are vital for planning a proficient reversible circuit. Adders are an essential segment of many figuring frame works. The main contri but ion of this dissertation is a set of design methodologies for the reversible realization of reversible 16-bit adder where the designs are based on the Peres gate. The proposed design is implemented on SPARTEN3 Microwind S and DSCS software.

Keywords— Microwind, Complex Gate, Energy, Logic Gate, Dissipation and Memory.

I. INTRODUCTION

In the gate designed in this paper using MEMS technology, there is no zero state or off state leakage current that is encountered in gates designed with CMOS transistors. Also, in this type of structure, there will be no uncontrolled behavior of transistors when the temperature rises, and the temperature effects of this structure are much less than CMOS. In addition, CMOS transistors respond poorly to ionizing radiation and therefore cannot operate in harsh environmental conditions. Therefore, electro-mechanical logic gates have overcome all these obstacles and therefore are of special importance for further exploration and analysis in this field. Also, due to the fact that in the CMOS structure of built-in gates consisting of a large number of transistors, the power consumption of this type of gates has increased, which is very optimized in our new structure. MEMS technology and the structure we are discussing will be able to perform several logical operations, but the important point is that the gate we want is just an XNOR logic gate and only this logical operation can be done with it and if need to other logical operations , A new structure can be designed and simulated for them, and by combining them, more complex functions or even different array networks can be achieved. Also, in the design structure section , we will first mention the possibility of multiple and even array connectivity of this designed gate, achieving gates with more than two inputs, as well as more complex functions and even the formation of a matrix neural network. However, due to the wide range of issues and the variety of logic functions, in this article we will only describe the basic structure of the two-input XNOR logic gate and examine the different conditions of this gate based on the possible variations in its input It should be noted that various methods for design in this structure such as piezoelectric structures, all-optical structures, etc. have been proposed and simulated so far, but the method we discuss, as mentioned earlier, is a combination of optical structure, mechanics And there is electrostatics, which we will describe in the following.

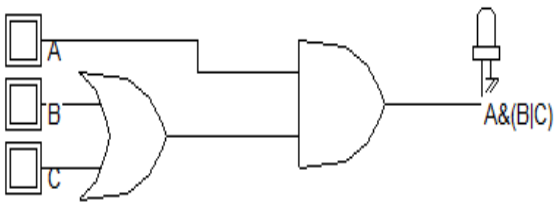

Figure.1a Comples Ciruit_01

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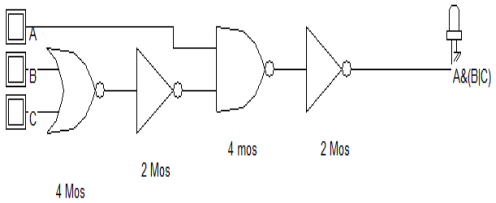

Figure.1a Comples Ciruit_02

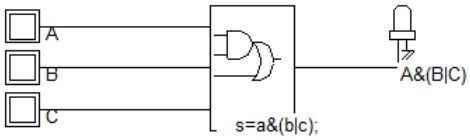

Figure.1a Comples Ciruit_03

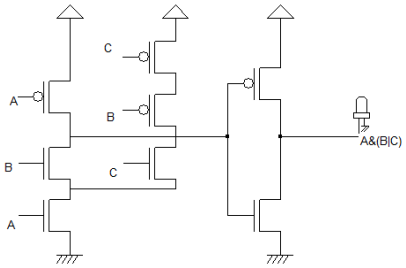

Figure.1a Comples Ciruit_04

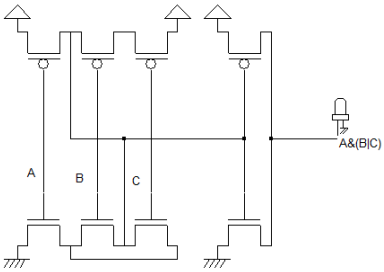

Figure.1a Comples Ciruit_05

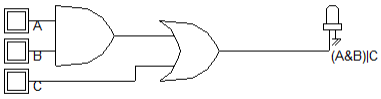

Figure.1b Comples Ciruit_01

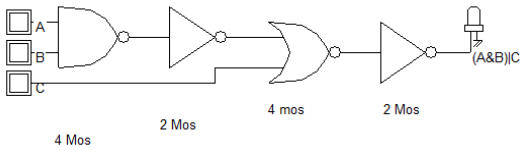

Figure.1b Comples Ciruit_02

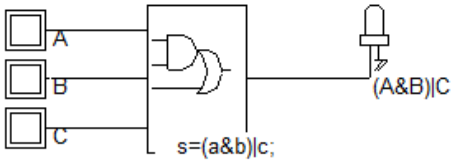

Figure.1b Comples Ciruit_03

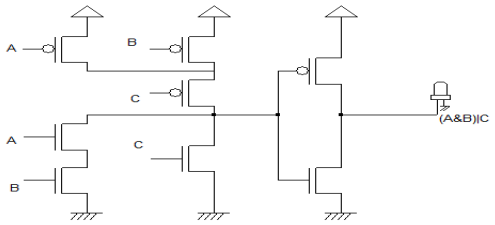

Figure.1b Comples Ciruit_04

II. LITERATURE SURVEY

Mohamadreza Eslami, et.al 2021 Design and Simulation of Optical XNOR Logic Gate Based on MEMS Technology, Prototypes of computers, or processors, were based almost exclusively on mechanical devices. Although electronic processors have become increasingly dominant over the past few decades, Recent advances in the technology of manufacturing 3D electromechanical components in micro and nano sizes have created new techniques for building complex microstructures that are of interest to researchers in new research In the field of mechanical computing. In this paper, we present a new XNOR logic gate design approach that can be built based on micro-electromechanical logic gates. One of the main advantages of this method is the ability to combine multi-physical as well as compatibility with the CMOS manufacturing process, as well as lower power consumption compared to logic gates consisting of several CMOS transistors. In this design, we have designed and simulated an XNOR logic gate using the multi-physics capability of Comsol software and as well as using optical, electronic, mechanical and electro-static physics, whose inputs will be both electrical and optical signals. In this paper, according to the above selected design, by modelling and simulating different input modes of this logic gate, we examine the effect of each mode on the output of the gate as well as other features such as structure life, power consumption and resonant frequency. The proposed gate structure has a resonant frequency of 46 kHz and is highly reliable because it can operate without mechanical connection of the MEMS operator to logic inputs **[01].**

Tie Mei et. al. 2021, A mechanical meta material with reprogrammable logical functions, Embedding mechanical logic into soft robotics, micro electromechanical systems (MEMS), and robotic materials can greatly improve their functional capacity. However, such logical functions are usually pre-programmed and can hardly be altered during in-life service, limiting their applications under varying working conditions. Here, we propose a reprogrammable technological metamaterial (ReMM). Logical computing is achieved by imposing sequential excitations. The system can be initialized and reprogrammed via selectively imposing and releasing the excitations. Realization of universal combinatorial logic and sequential logic (memory) is demonstrated experimentally and numerically. The fabrication scalability of the system is also discussed. We expect the ReMM can serve as a platform for constructing reusable and

multifunctional mechanical systems with strong computation and information processing capability **[05].**

Yuanping Song,et al 2019, Additively manufacturable micro-mechanical logic gates, Early examples of computers were almost exclusively based on mechanical devices. Although electronic computers became dominant in the past 60 years, recent advancements in three-dimensional micro-additive manufacturing technology provide new fabrication techniques for complex microstructures which have rekindled research interest in mechanical computations. Here we propose a new digital mechanical computation approach based on additively manufacturable micro-mechanical logic gates. The proposed mechanical logic gates (i.e., NOT, AND, OR, NAND, and NOR gates) utilize multi-stable micro-flexures that buckle to perform Boolean computations based purely on mechanical forces and displacements with no electronic components. A key benefit of the proposed approach is that such systems can be additively fabricated as embedded parts of micro architected met materials that are capable of interacting mechanically with their surrounding environment while processing and storing digital data internally without requiring electric power **[02].**

Sally Ahmed et al 2019, A Compact Adder and Reprogrammable Logic Gate Using Micro-Electromechanical Resonators With Partial Electrodes, The design principles and experimental demonstration of a compact full adder along with a reprogrammable 4-input logic gate are presented. The proposed solution for implementation of digital circuits is based on a clamped–clamped micro-beam resonator with multiple split electrodes, in which the logic inputs tune the resonance frequency of the beam. This technique enables re-programmability during operation, and reduces the complexity of the digital logic design significantly; as an example, for a 64-bit adder, only 128 micro resonators are required, compared to more than 1500 transistors for standard complementary metal–oxide–semiconductor (CMOS) architectures. We also show that an optimized simulated micro-resonator-based full adder is 45 times smaller than a CMOS mirror adder in 65-nm technology. While the energy consumption of this early generation of micro-resonator logic gates is higher than the CMOS solutions, we show that by careful device optimization and shrinking of the dimensions, femtojoules energy consumption and MHz operation, required by Internet of Things applications, are attainable **[04].**

Saad Ilyas et. al. ,2017, Multi-function and cascadable mems logic device, We present a reprogrammable Micro electromechanical systems (MEMS) logic device that can perform the fundamental logic gate AND, a universal logic gate NAND, and a tristate logic gate using mixed-frequency excitation. The concept is based on exciting combination resonances due to the mixing of two or more input signals. The device vibrates at two steady states; a high state when the combination resonance is activated and a low state when no resonance is activated. These vibration states are assigned to logical value 1 or 0 to realize these logic gates. Using AC signals to drive the resonator and to execute the logic inputs unifies the input and output wave forms of the logic device, thereby opening the possibility for cascading among logic devices. Moreover, the ability to perform these logic operations at any input frequency using frequency mixing techniques allows for overcoming the limitation of having a fixed operating frequency. These characteristics of such logic devices lay down the basis to achieve complex computing operations **[03].**

Gopi Chand Naguboina et.al. 2017 "Design and Synthesis of Combinational Circuits Using Reversible Decoder in Xilinx", reversible rationale is the rising field for inquire about in exhibit period. The point of this paper is to acknowledge diverse kinds of combinational circuits like full-viper, full- subtractor, multiplexer and comparator utilizing reversible decoder circuit with least quantum cost. Reversible decoder is composed utilizing Fredkin doors with least Quantum cost. There are numerous reversible rationale doors like Fredkin Gate, Feynman Gate, Double Feynman Gate, Peres Gate, Seynman Gate and some more. Reversible rationale is characterized as the rationale in which the number yield lines are equivalent to the quantity of info lines i.e., the n-information and k-yield Boolean capacity F(X1, X2, X3,… ,Xn) (alluded to as (n, k) work) is said to be reversible if and just in the event that (I) n is equivalent to k and (ii) each info design is mapped extraordinarily to yield design **[06].**

Marcin Bryk et.al. 2016, **"Encryption using reconfigurable reversible logic gate and its simulation in FPGAs"**, recently an approach to encryption/decryption based on using reversible logic circuits has been proposed. The reason for this is that conventional microelectronic technologies are reaching their limits. On the other hand, reversible logic circuits can decrease energy dissipation theoretically to zero. This paper presents a solution to designing encryption schemes based entirely on reversible logic. In our solution a building block of an encryption scheme is a cascade of 4-input reversible gates. In this way the building block can perform any reversible 4-variable function. For this purpose a reconfigurable reversible gate has been proposed. The design of such a reconfigurable gate built from standard reversible gates, i.e. NOT, CNOT, Toffoli and Fredkin gates, is presented. In the paper a complete scheme for encryption/decryption of 8-bit data is described using VHDL language and its quantum cost is calculated. Simulation and verification of this scheme in FPGAs conclude the paper **[07].**

Lafifa Jamal et.al. 2015 ,"Design and Implementation of a Reversible Central Processing Unit", Quantum computing necessitates the design of circuits via reversible logic gates. Efficient reversible circuit can be constructed by achieving low ancilla count, reducing logical depth and lowering Quantum costs. Generalized Peres gates have recently been realized with very low Quantum Cost (QC) by utilizing Quantum rotation gates. This is utilized in recent literature for efficient reversible circuit constructions for symmetric Boolean functions. In this paper, we extend this line of

construction further by demonstrating efficient realization of adder circuits. In particular, we revisit the adder construction of Vedral, Barenco and Eckert to show that improvement of gate count and QC is achievable by exploiting a construction based only on Peres gates **[08].**

Junchao Wang et.al. **2014, "A Carry look ahead adder designed by reversible logic"** , this paper says that a lot of attentions have been attracted by the reversible logic due to the characteristic of zero energy dissipation. Reversible logic can be applied in fields such as low power CMOS circuits, quantum computation and DNA computing. In this paper, the author proposed a 16 bit carry look-ahead adder is constructed by four 4 digits groups based on the theory of reversible logic, which has the advantages of theoretical zero power dissipation and high efficiency **[09].**

James Donald et.al. 2008 "Reversible logic synthesis with fredkin and peres gates" in this paper it has been realized that quantum computing is one of the latest technologies using reversible logic. It is observed that increasing growth of transistor density, power consumption will reach their limits in conventional technologies. In conventional Circuits during the logic operations bits of information is erased resulting dissipation of energy in significant amount. Thus, if Circuits are designed so that information bits can be preserved, the power use can be reduced. In case of reversible logic computation, the information bits are not lost. We can use reversible logic technology for minimizing the power consumption, heat dissipation, increasing speed etc. This paper describes various logic gates based on reversible logic like Toffoli, Peres, Fredkin, and Feynman etc. A comparative between classical and quantum logic gates is also given on various parameters along with limitations of conventional computing **[10].**

III. PROBLEM STATEMENT

As seen from the literature survey the importance of Complex logic in digital system design the approximation zero power is lost in reversible logic, and by studying different reversible logic gate it is found that peres gate has the lowest number of quantum cost so in this thesis implementation of Complex Logic Gate has been implemented using simple multiple Gate.

IV. MATHEMATICAL MODELLING & CONTROL OF DVR

AOI and OAI complex gates :- A demonstration of a few complex logic gates, namely the OR-AND-INVERT and OR-AND-INVERT gates. Click the input switches to toggle the corresponding input value between 0 and 1, and watch the resulting behaviour. You can also use shift+click to toggle the input value between the states 0, 1, Z (tri-state, not driven) and X (undefined). The names of these gates are derived from their AND-OR-INVERT and OR-AND-INVERT structure and the number of inputs of the first level gates. To give another example, an OAI222 gate (not shown in the applet) is equivalent to three two-input OR gates that drive a three-input NAND gate. Complex gates are often used in CMOS VLSI chip design because they can be realized very efficiently, based on clever combinations of series- and parallel-connected transistors. For example, the AOI33 gate can be built using just 12 transistors, while the corresponding discrete realization would require 4 transistors for the NOR gate, and 8 transistors for each AND3 gate for a total of 20 transistors - almost twice as expensive and twice as slow.

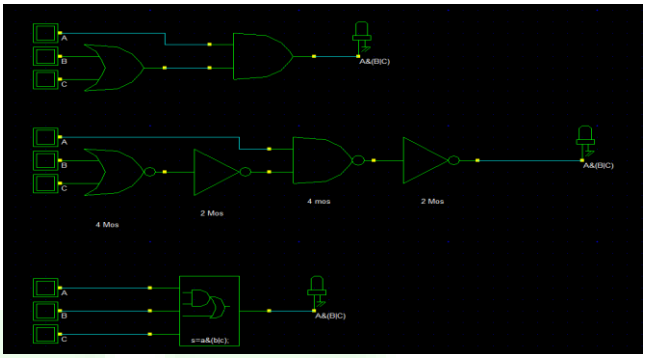

Figure 1: Complex Gate Design View_01

The Complex Gate View the fuction of A&(B+C) Show in the figure

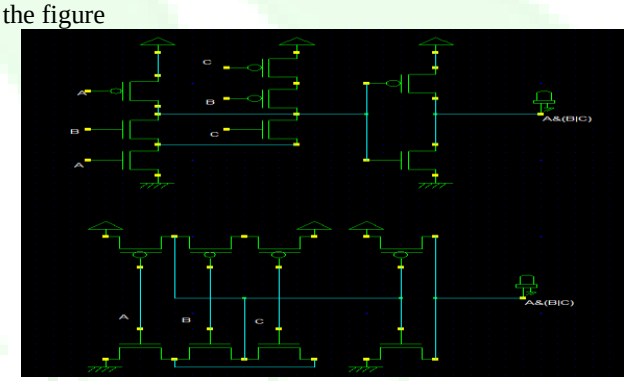

Figure 1: Complex Gate Design View_02

The Complex Gate CMOS View the fuction of A&(B+C) Show in the figure .

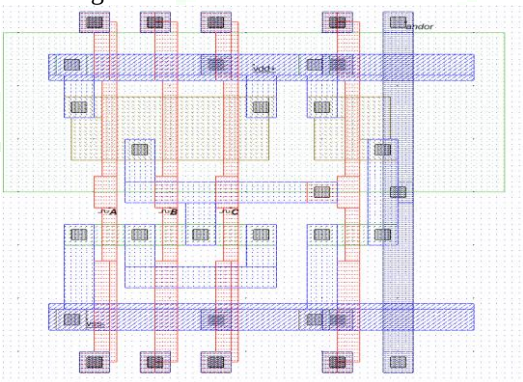

Figure 2 fuction of A&(B+C)

V. RESULTS AND DISCUSSION

V.1 Voltege Vs Time Graph:- Volteg Vs Time Graph show in the Figure 5.1. On this simulation power used is 9.165µw.

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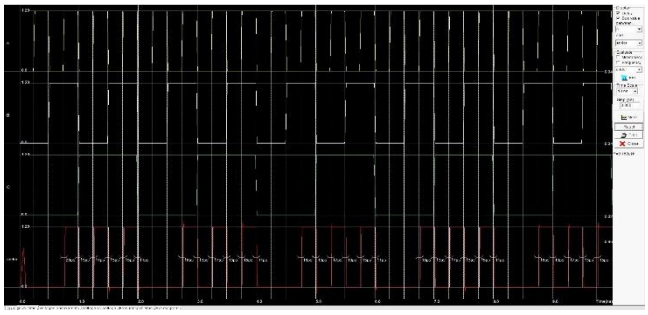

Figure 2 Voltage Vs Time Graph

V.2 Voltege Vs Current Graph:- Voltege Vs Current Graph show in the Figure 5.2. On this simulation power used is 9.165µw.

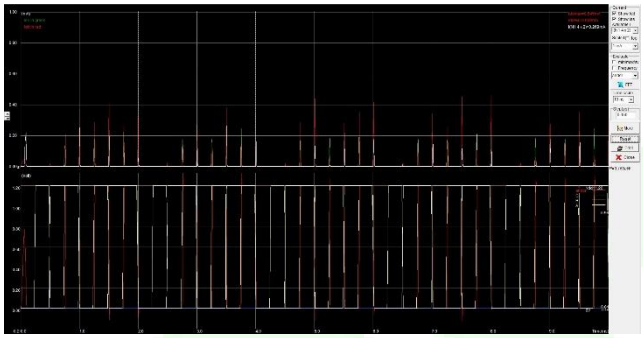

Figure 3 Voltege Vs Current Graph

V.3 Voltege Vs Voltage Graph:- Volteg Vs Time Graph show in the Figure 5.3. On this simulation power used is 9.165µw.

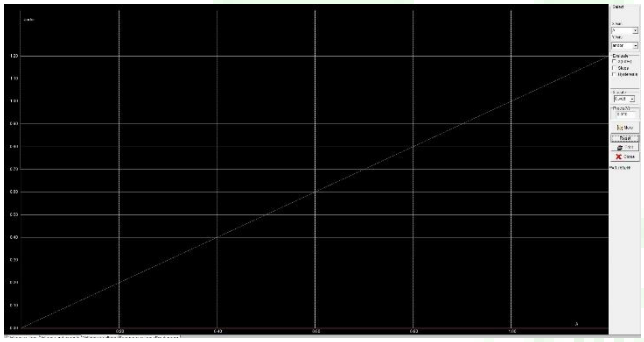

Figure 4 Voltege Vs Voltage Graph

V.4 Frequency Vs Time Graph:- Frequency Vs Time Graph show in the Figure 5.4. On this simulation power used is 9.165µw.

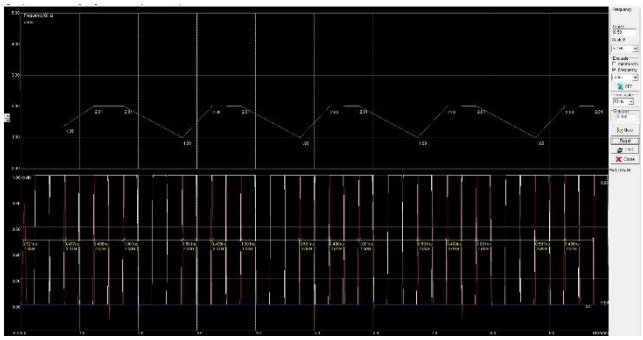

Figure 5 Frequency Vs Time Graph

V.5 Eye Diagram:- Eye Diagram Graph show in the Figure 5.5. On this simulation power used is 9.165µw.

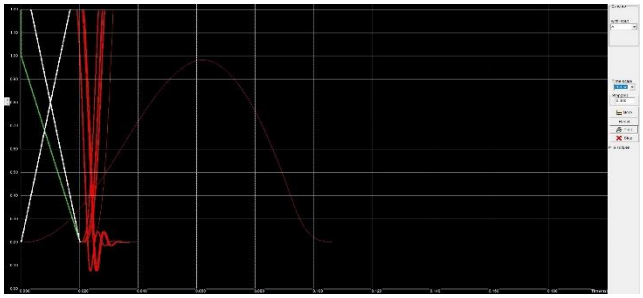

Figure 5 Eye Diagram

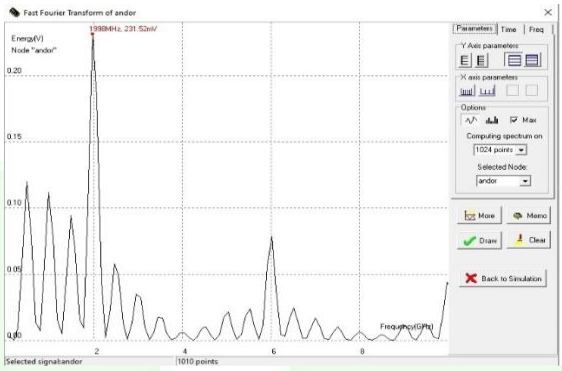

Figure 6 FFT Analysis of Circuit

VI. CONCLUSION

As we realize that the rudiments of reversible figuring depend on the relationship between entropy, heat move between atoms in a framework, the likelihood of a quantum molecule possessing a specific state at any given time, and the quantum electrodynamics between electrons when they are in close nearness. The essential guideline of reversible registering is that a bijective gadget with an indistinguishable number of information and yield lines will produce a computing environment where the electrodynamics of the system allow for calculation of all future states based on known past states, and the system reaches every possible state, resulting in no heat dissipation.

Hence in this design we have proposed a design to calculate the power that is analogous to heat dissipation and to compare the delay and increase the number of logical arithmetic operation. The numbers of steps followed in this thesis are as under:

1. Two highly programmable, low-cost and low-delay 4*4 reversible logic gates were presented, verified and compared to similar logic structures already published.
2. The proposed modified fredkin gate as the best existing 4×4 reversible gates in terms of cost, delay and logical output calculations.
3. The gates were then implemented in reversible arithmetic logic units. These new decoder, multiplier designs are advantageous to previously published work in implementations that favor low delay and high logical calculation output, which is

desirable for realization of a reversible central processing unit.

4. The proposed designs are then integrated in the design of a novel reversible combinational circuit.

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