http://www.jctjournals.com

ISSN(ONLINE):2278 - 3814

Volume-12, Issue-11, November 2023

JOURNAL OF COMPUTING TECHNOLOGIES (JCT)

International Journal

Page Number: 01-05

Implementation of Area Optimized Flash ADC Layout by Using 250nm Technology

[1]*Shubham Junghare*, [2]*Prof. Nishi Pandey* [3]*Prof. Abhishek Agwekar*
[1]*M.Tech Scholar,* [2]*Assistant Professor,* [3]*Head of department (HOD)*
[1, 2, 3]*TIEIT , Bhopal, M.P., India*

shubhamjunghare09@gmail.com, nishi.pandey@trubainstitute.ac.in, abhiagwekar@gmail.com

ABSTRACT :- ***Analog to Digital Converter (ADC) plays an important role in digital signal processing systems. The main challenges of designing ADC for system on chip applications are high speed, low voltage, and low power consumption. Reducing the power consumption is a major concern in a portable device. Low power techniques are applied to prolong the battery life of a system. Similarly ADCs also require a low power technique in the design to reduce the total power consumption of ADC. Speed, power dissipation and resolution are the three crucial parameters the design of any ADC which cannot be changed once the design is complete. In wireless and mobile communication applications require a high speed ADC with low resolution. In these applications, flash ADC is the most suitable ADC because of its parallel operation. The complete conversion is done in a single cycle with the help of a large number of comparators.***

Keywords: Unit commitment, Dynamic Programming, Fuel cost, Voltage stability, Economic dispatch

I. INTRODUCTION

An ADC is a very important feature that converts an analog signal to a digital signal. It provides the bridge between the analog and digital world. There are different types of ADCs pipelined ADC, Sigma-delta ADC, counter type ADC, etc which are affected by noise and power consumption. With the implementation of various technologies in the analog to digital circuits, the noise and power consumption can vary simultaneously [7]. There are three types of technologies used in data converters which are CMOS technology, bipolar technology, and gallium arsenide technology (GaAs) [4]. Among this CMOS technology having a high noise immunity and low static power consumption. One problem with TIQ is that is noise susceptibility [5]. TIQ has a single-ended input, the comparator is very sensitive to power supply noise and power supply voltage. To overcome this problem, we use a new comparator called Quantum Voltage (QV). It does not use the resistor ladder circuit. The QV comparator is derived from differential comparator [5]. There are different types of encoder like Wallace tree encoder, PLA/ROM and XOR encoders. We use a pseudo-logic encoder which directly converts the thermometer code to binary code. It also provides high coversion data rates while maintaining low power consumption [8].

II. LITERATURE REVIEW

Bang-Sup Song, et.al. **"A 1 V 6 b 50 MHz current-interpolating CMOS ADC" VLSI Circuits, 1999[1]**, S.A current-interpolation technique is used to implement a 6b 50 MHz ADC operable with a single battery cell as low as 0.9 V without charge pumping. The prototype chip, fabricated in a 0.35 μm standard digital process, occupies an area of 2.4 mm×2 mm, and consumes 10 mW each in analog and digital supplies, respectively [1].

Ono, K. Shimizu, H *et.al.* "A 6bit 400Msps 70mW ADC using interpolated parallel scheme" VLSI Circuits Digest of Technical Papers, 2002[2], The design of a low power 6bit, 400Msps, 1.8V CMOS ADC is presented. This ADC is based on interpolated parallel architecture in which the transistor sizes are optimized to achieve the required linearity and simultaneously minimize the power consumption. When operated at 400Msps with 1.8/2.4V power supply the ADC dissipates 70mW. The ADC is fabricated in a 0.18/spl mu/m CMOS process [**3].**

Paulus, C. Bluthgen, *et.al.*. "A 4GS/s 6b flash ADC in 0.13 /spl mu/m CMOS" Digest of Technical Papers. 2004[3], A 4GS/s 6b flash ADC with 8b output is presented realized in a 0.13 /spl mu/m standard CMOS technology. The outputs of 255 small-area comparators with

comparatively large input offsets are averaged by a fault tolerant thermometer-to-binary converter. The ADC uses an on-chip low jitter VCO for clock provision and consumes 990mW at a single supply voltage of 1.5V [3].

Hayun Chung, *et.al.*"A 7.5-GS/s 3.8-ENOB 52-mW flash ADC with clock duty cycle control in 65nm CMOS" Browse Conference Publications, 2009[4], A 7.5-GS/s 4.5-bit analog-to-digital converter (ADC) in 65nm CMOS is presented. A two-stage track-and-hold (TAH) with clock duty cycle control reduces bandwidth requirements on the slow TAH output to enable high sampling rates with low power consumption. The 7.5-GS/s flash ADC consumes 52-mW and occupies 0.01-mm2. Clock duty cycle control improves ENOB from 3.5 to 3.8 with an input sinusoid at the Nyquist frequency. [5] Y.-S. Shu "A 6b 3GS/s 11mW Fully Dynamic Flash ADC in 40nm CMOS with Reduced Number of Comparators" VLSI Circuits (VLSIC), 2012[5]Symposium, A 6b 3GS/s fully dynamic flash ADC is fabricated in 40nm CMOS and occupies**0.**021mm2. Dynamic comparators with digitally controlled built-in offset are realized with imbalanced tails. Half of the comparators are substituted with simple SR latches. The ADC achieves SNDRs of 36.2dB and 33.1dB at DC and Nyquist, respectively, while consuming 11mW from a 1.1V supply [4].

V.H.-C. Chen *et.al.*"An 8.5mW 5GS/s 6b Flash ADC with Dynamic Offset Calibration in 32nm CMOS SOI" VLSI Circuits (VLSIC), 2013[6] Symposium, This paper describes a 5GS/s 6bit flash ADC fabricated in a 32nm CMOS SOI. The randomness of process mismatch is exploited to compensate for dynamic offset errors of comparators that occur during high speed operation. Utilizing the proposed calibration, comparators are designed with near-minimum size transistors and built-in reference levels. The ADC achieves an SNDR of 30.9dB at Nyquist and consumes 8.5mW withFoM of 59.4fJ/conv-step. **[6].**

R. Komar, M. *et.al*, "A 0.5 V 300µW 50MS/s 180nm6bit Flash ADC using inverter based comparators," 2012, This paper presents an ultralow power 6 bit Flash ADC designed in 180 nm CMOS technology for ultralow power applications. The design uses inverter based comparators to reduce the silicon area and power requirement. A novel clock delaying technique is used to power on the three stages of the comparator which work in series. This reduces the power consumption and increases speed of operation. Fat tree architecture is used to design the digital encoder. The power supply used for the design is 0.5 V and the sampling rate is 50 MS/s. The design consumes ultralow power of 600 µW and spans a very small area of 0.164 mm2. In literature this is found to be the lowest for 6 bit ADCs in 180 nm with sampling frequency of 5 MS/s or above. The SNDR remains above 31.5 dB in the whole input frequency range of 0 to 25 MHz. The ADC has maximum DNL of 0.85 LSB and maximum INL of 1 LSB. The FOM of the ADC is found to be 0.39 pJ/conv**[7]**.

III . PROPOSED METHODOLOGY

Tanner Eda software: Tanner EDA tools for analog and mixed-signal ICs and MEMS design offers designers a seamless, efficient path from design capture through verification. Our powerful, robust tool suite is ideal for applications including Power Management, Life Sciences / Biomedical, Displays, Image Sensors, Automotive, Aerospace, RF, Photovoltaics, Consumer Electronics and MEMS. In this we use S-Edit, T-Edit and W-Edi.

3.1 Introduction

3.1.1 S-Edit: S-Edit™ is an easy-to-use PC-based design environment for schematic capture. It gives you the power you need to handle your most complex full custom IC design capture. S-Edit is tightly integrated with Tanner EDA's T-Spice™ simulation, L-Edit™ layout, and HiPer™ verification tools. S-Edit helps you meet the demands of today's fast-paced market by optimizing your productivity and speeding your concepts to silicon. Its efficient design capture process integrates easily with third-party tools. S-Edit enables you to explore design choices and provides an easy-to-use view into the consequences of those choices. A faster design cycle gives you more flexibility in moving to an optimal solution, freeing up more time and resources for process corner validation. The results are less risk downstream, higher yield, and quicker time to market.

IV. ARCHITECTURAL DETAILS

4.1 Architectural Details Flash ADCs are made by cascading high-speed comparators. A 3-bit flash converter shown in **Figure 1** flash ADC block diagram. For an N-bit converter, the tota l number of flash or parallel comparators 2N-1. In this ADC ,2Nresistors and 1-priority encoder type (2N*n) are needed. A resistive-divider with 2N resistors provides the reference voltage. The reference voltage for each comparator is one least significant bit (LSB) greater than the reference voltage for the comparator immediately below it. Comparator produces a 1 when its analog input voltage is higher than the reference voltage applied to it. Otherwise, the comparator output is 0.

4.2 Operation

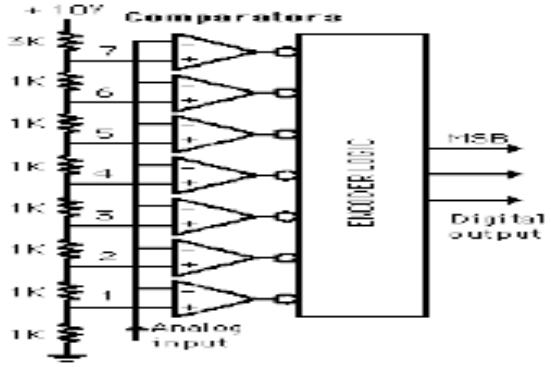


Fig 4.1 : 3-bit flash converter

ISSN(ONLINE):2278 - 3814

As thetruth table in fig 2, it is clear that 1-pariority encoder gives the output as digital form. With VA<1V, all the comparators outputC1 toC7 will be high. With VA>1V, one or more of the comparator output will be LOW. The comparator outputs are fed into active-LOW priority encoder that generates a binary output corresponding to the highest numbered comparator output that is LOW. For example, when VA =3.5V, outputs C1 ,C2and C3 will be LOW and all others will be HIGH

.

4.3 COMPARATOR: - **N-Channel MOS (NMOS):-**It is used in most of the memory and microprocessor in computer. N-channel is faster than PMOS.NMOS conducts whenever input is high. **P-Channel in MOS (PMOS):-**It is used FETs having heavily doped P-channel. PMOS conducts whenever inputs are LOW.it is called PULL Up Network.This is the final layout design. In this layout, there are PMOS and NMOS of different parameters and blue area is a capacitor of range 0.5pf and red color is depict resister. Routing of this layout is done according to the schematic as shown below.

A comparator was defined above as a circuit that has a binary output whose value is based on a comparison of two analog inputs. The output of the comparator is high when the difference between the non inverting and inverting inputs is positive, and low when this difference. The

accuracy of such comparators, which is defined by its offset, along with power consumption, speed is of keen interest in achieving overall higher performance of ADCs. In Fig.1.1 block diagram has been shown of the conventional three stage comparators in which the first stage is denoted as the main preamplifier, the second stage is a simple gain stage which is also considered as isolating block between preamplifier and latch, and the final stage is attached to output latch [2]. Cascading three blocks requires larger area and power consumption. Dynamic comparators are being used in today‘s A/D converters extensively because these comparators are high speed, consume lesser power dissipation, having zero static power consumption and provide full-swing digital level output voltage in shorter time duration. Back-to-back inverters in these dynamic**.**

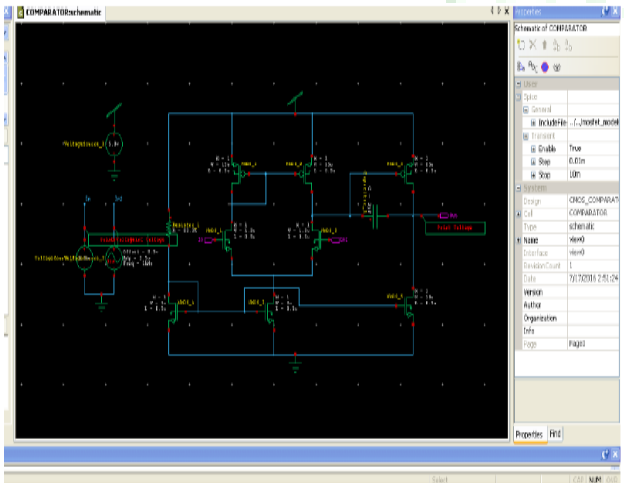


Fig 3.2 Ckt Diagram

comparators provide positive feedback mechanism which converts a smaller voltage difference in full scale digital level output. However, an input-referred latch offset, resulting from the device mismatches such as threshold voltage, current factor β (=μ.CoxW/L) and parasitic node capacitance and output load capacitance mismatches, limits the accuracy of such comparators [3]

.

4.4 INVERTER: Inverter is made using a PMOS and a NMOS having their gate common. PMOS is attached to VDD and NMOS to GND as shown below. The inverter is truly the nucleus of all digital designs. Once its operation and properties are clearly understood, designing more intricate structures such as NAND gates, adders, multipplers, and microprocessors is greatly simplified. The electrical behavior of these complex circuits can be almost completely derived by extrapolating the results obtained for inverters. The analysis of inverters can be extended to explain the behavior of more complex gates such as NAND, NOR, or XOR, which in turn form the building blocks for mod- ules such as multipliers and processors. In this chapter, we focus on one single incarnation of the inverter gate, being the static CMOS inverter — or the CMOS inverter, in short. This is certainly the most popular at present, and therefore deserves our special attention.

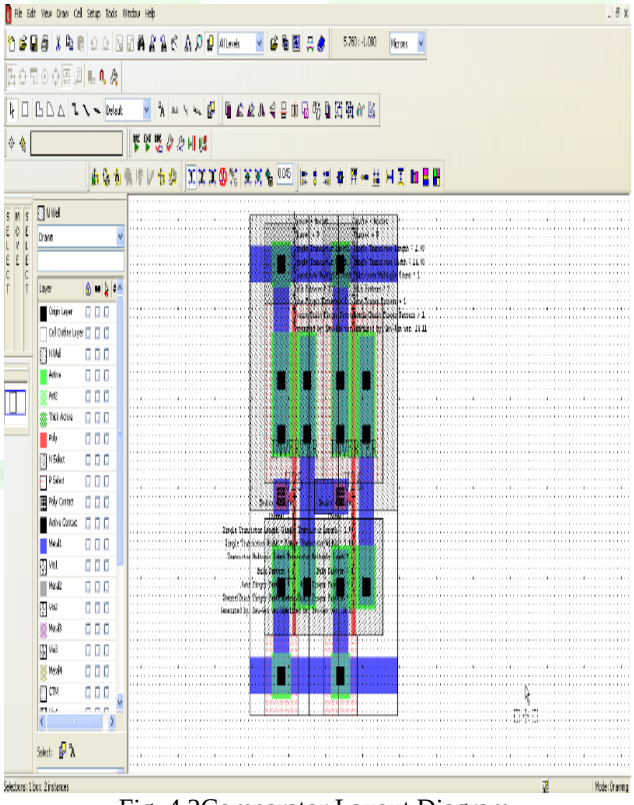


Fig. 4.2Comparator Layout Diagram

4.5 PRIORITY ENCODER:- This is the modified version of simple encoder which is eliminates the drawback of encoder (when more than one input is activate at a time). A _priority encoder‘ includes the necessary logic to ensure that when two or more inputs are activated the output code

ISSN(ONLINE):2278 - 3814

will correspond to the _highest number of input‘. A priority encoder is a circuit or algorithm that compresses multiple binary inputs into a smaller number of outputs. The output of a priority encoder is the binary representation of the original number starting from zero of the most significant input bit. They are often used to control interrupt requests by acting on the highest priority encoder.If two or more inputs are given at the same time, the input having the highest priority will take precedence.[1] An example of a single bit 4 to2 encoder is shown, where highest-priority inputs are to the left and "x" indicates an irrelevant value - i.e. any input value there yields the same output since it is superseded by higher-priority input. The output V indicates if the input is valid.

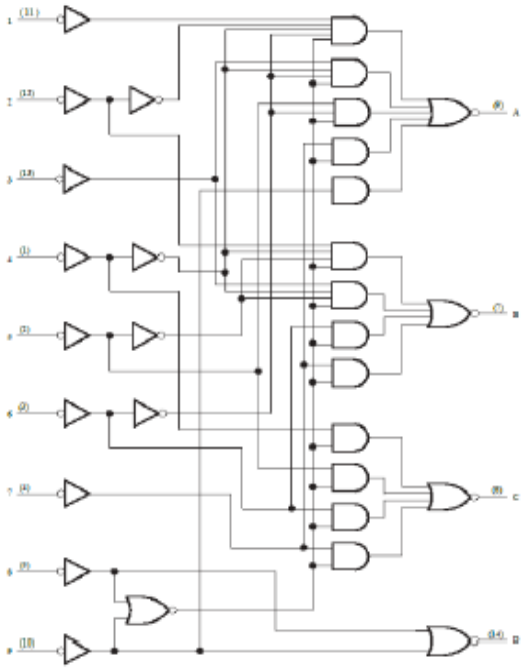


Fig 4.38:3 encoder using inverter AND gate and NOR gate.

Priority encoders are available in standard IC form and the TTL 74LS148 is an 8-to-3 bit priority encoder which has eight active LOW (logic ―0‖) inputs and provides a 3-bit code of the highest ranked input at its output. Priority encoders output the highest order input first for example, if input lines ―D2―, ―D3‖ and ―D5‖ are applied

V. SIMULATION RESULT

5.1 Simulation Result

The test comparator Layout is designed in a 250 Nano meter with a total area 7.73712*10^-5 mm Square.
MBB-0.025965*0.03609 mm
Density-8.25665%

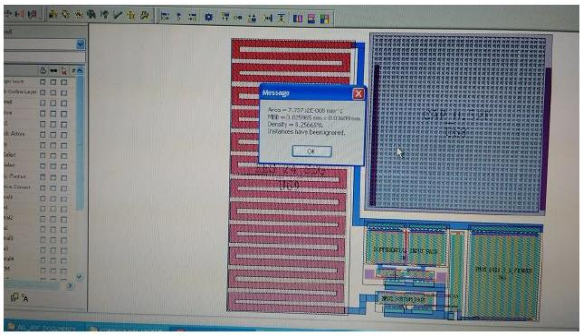


Fig 5.1 Result From

From this paper it has been established that a complete fully customized standard cell layout is possible of a FLASH ADC is possible on a 250 nm standard CMOS process. ADc requiresfollowing circuits which are made and simulation resultsa of which are verified

 Comparator-comparator compares two voltage level and gives output. Here we have given analog signal as input and we get digital signal as output depending on clock

- Priority encoder-it will gives priority to given input and corresponding output is given
- Buffer-it helps to achieve proper level of output as well introduce delay in circuit
- Inverter-to invert input. After verification of result of each block, layout is done for each block.

5.2 Comparator Analysis & Related Work:- N-Channel MOS (NMOS):-It is used in most of the memory and microprocessor in computer. N-channel is faster than PMOS.NMOS conducts whenever input is high. **P-Channel in MOS (PMOS):-**It is used FETs having heavily doped P-channel. PMOS conducts whenever inputs are LOW.it is called PULL Up Network. This is the final layout design. In this layout, there are PMOS and NMOS of different parameters and blue area is a capacitor of range 0.5pf and red color is depict resister. Routing of this layout is done according to the schematic as shown below.

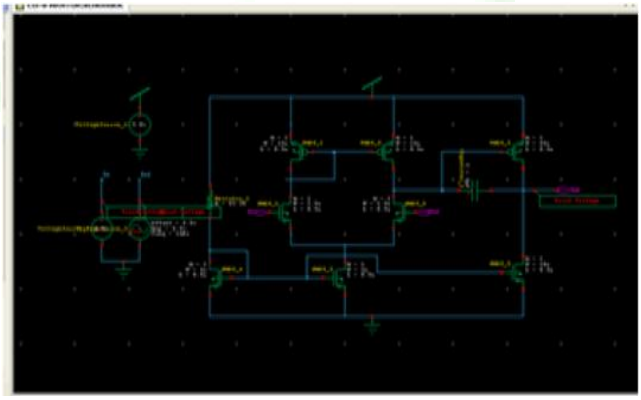
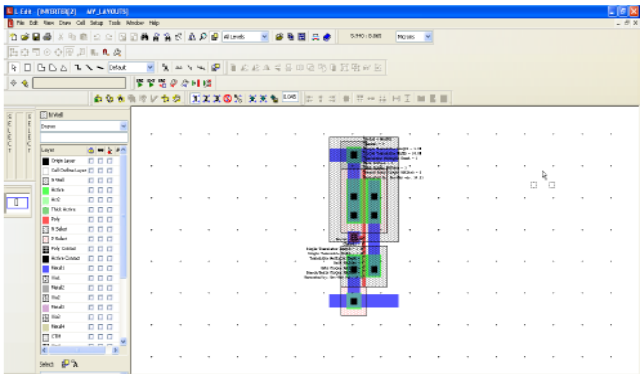


Fig 5.2 Ckt diagram

5.3 INVERTER: Inverter is made using a PMOS and a NMOS having their gate common. PMOS is attached to VDD and NMOS to GND as shown below

ISSN(ONLINE):2278 - 3814



5.4 Comparator Layout This is the final layout design. In this layout, there are PMOS and NMOS of different parameters and blue area is a capacitor of range 0.5pf and red color is depict resister. Routing of this layout is done according to the schematic as shown below.

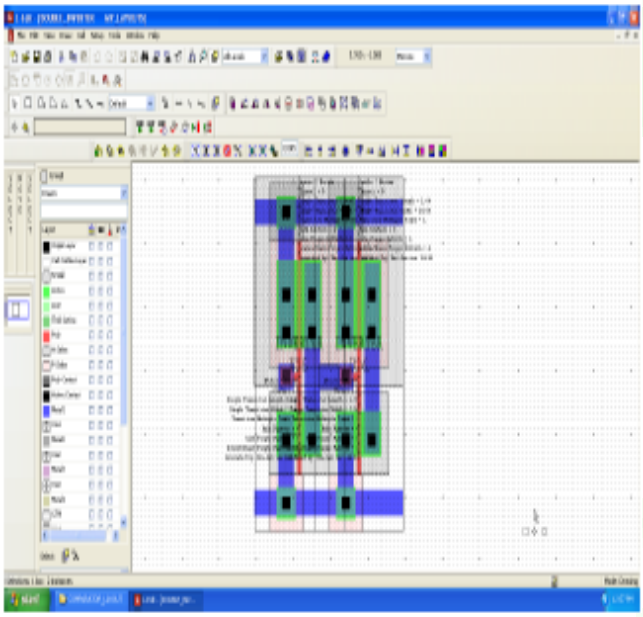


Fig. 5.4 Comparator Layout Diagram

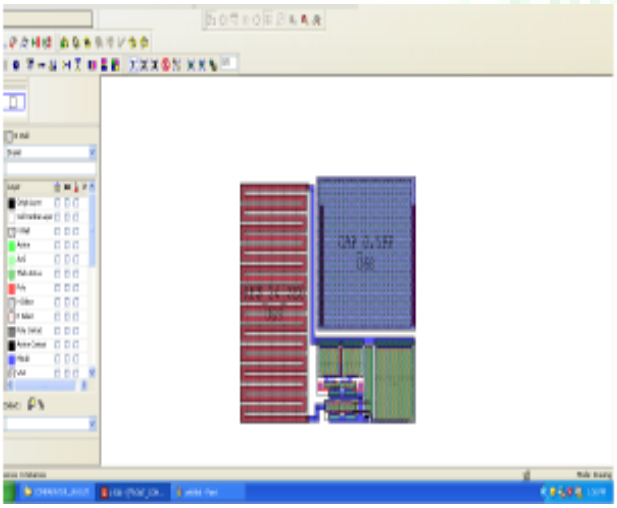
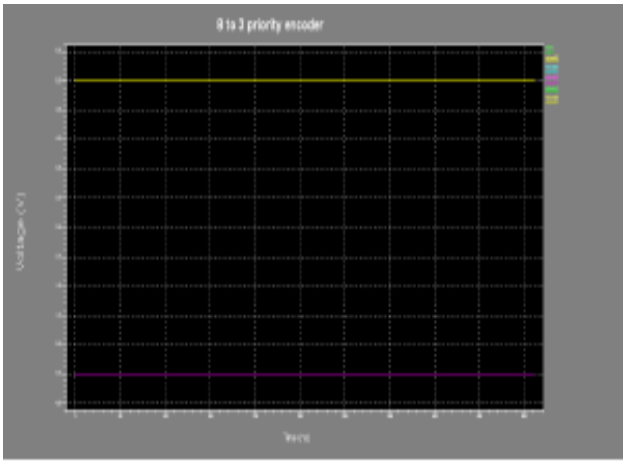


Fig. 5.5Waveform of layout.

5.6 8:3 encoder using inverter AND gate and NOR gate is shown above. 8:3 Priority Encoder Layout:-



5.6.1 16:4 Priority Encoder Layout:- priority encoder is made from 8:3 encoder using‖ IC 74147‖.

VI. CONCLUSION AND FUTURE WORK

A new dynamic ADC which shows lower power consumption and high speed than the conventional dynamic latched ADCs has been designed. With two additional inverters inserted between the input- and output-stage of the conventional double tail dynamic ADC, the gain preceding the regenerative latch stage was improved and the complementary version of the output-latch stage, which has bigger output drive current capability at the same area, was implemented. Because ADCs have only two output states, their outputs are near zero or near the supply voltage. Here, clocking technique has been used to switch faster at intermediate nodes and reduces the power dissipation. So, a PMOS used between nodes. When clock is zero, then both nodes should be at same potential (by shorted **the nodes using PMOS at clock=0). Here, the** W/L ratios also arranged of each transistor to reduce the power consumption in the ADC. This process is carried out at 5GHz clock frequency and 180nm technology.

As mentioned earlier, since the proposed fully dynamic latched ADC can be optimized for either the minimum kickback noise voltage or the maximum load drivability at a limited area according to the design specification, searching for the most suitable application can be one topic for the future works. In addition, kickback noise cancellation techniques can be considered for further reduction of the kickback noise voltage.

REFERENCES

[1] Design of A Simple Digital ADC Using Only Digital Blocks and Delay Element Circuit‖, Shakti Prasad Senapati, IEEE International Conference On Recent Trends In Electronics Information Communication Technology, May 20-21, 2016, India

[2] KuMoon Skyler Weaver, Member, IEEE, Benjamin Hershberg, Member, IEEE, and Un-, Fellow, IEEE Digitally Synthesized Stochastic Flash ADC Using Only Standard Digital Cells IEEE Transactions On

Circuits And Systems-I:Regular Papers,VOL.61, NO.1, JANUARY 2014.

[3] S. Setoodeh, R. Mansour, and D. Gupta, ―Multi-layer low temperature superconducting K-band filter and diplexer design,‖ in Proc. IEEE MTT-S IMS Dig., Jun. 2–7, 2013, pp. 1, 4.

[4] H. Suzuki, M. Oikawa, K. Nishii, and M. Hidaka, ―Investigation of a 5-bit flash-type SFQ A/D converter using 10 kA/cm2 niobium process and locally isolated grounds, IEEE Trans. Appl. Supercond., vol. 23, no. 3, Jun. 2013, Art. ID. 1400805.

[5] A. Inamdar, A. Sahu, J. Ren, A. Dayalu, and D. Gupta, ―Flash ADC comparators and techniques for their evaluation,‖ IEEE Trans. Appl. Supercond., vol. 23, no. 3, Jun. 2013, Art. ID. 1400308.

[6] H.Tang, H.Zhao, X.Wang, L.Lin, Q .Fang,J. Liu,A. Wang,S. Fan,B. Zhao ,Z.Shi, and Y.Cheng, ―Capacitive interpolated flash ADC design technique,‖inProc.2010 Int. So C Design Conf.(ISOCC),Nov.2010, pp. 166–169.

[7] S .Weaver et.al. "Stochastic flash analog to digital conversion",IEEETrans.CircuitsSyst.I,vol.57,pp.2825 –2833,Nov.2010.

[8] S. Weaver, B. Hershberg ,and U.Moon,― ENOB calculation for ADCs with input-correlated quantization error using a sine Proc .2010 Int. Conf. Microelectronics(ICM),Dec.2010,pp.5–8.

[9] S.Wolf, Silicon Processing for the VLSI Era:Deep-Submicron Process Technology. Sunset Beach, CA, USA: Lattice Press, 2002.

[10] M.Shaker,S.Gosh,andM.Bayoumi,―A1-Gs/s6 bit flashADCin90nmCMOS,‖inProc.52ndIEEEInternationalMidwestSymp.Circuits and Systems, MWSCAS‘09, Aug. 2009, pp. 144–147.

[11] H.Tang,H.Zhao,X.Wang,L.Lin,Q.Fang,J.Liu,A.Wang,S.Fan,B.Zhao,Z.Shi,andY.Cheng,―CapacitiveinterpolatedflashADCdesigntechnique,‖inProc.2010Int.SoCDesignConf.(ISOCC),Nov.2010, pp. 166–169.

[12] S. B. Kaplan et al., ―A superconductive flash digitizer with on-chip memory, IEEE Trans. Appl. Super cond., vol. 9, no. 2, pp. 3020–3025, Jun. 1999.

[13] M. Maruyama, H. Suzuki, Y. Hashimoto, and M.Hidaka,―A flash AD Cusing Complementarily Combined SQUIDs, IEEE Trans. Appl. Super cond., vol. 19, pp. 680–684, Jun. 2009.

[14] H. Suzuki etal., Design and demonstrationo fa5-bit flash-type SFQADC integrated with error-correction and interleaving circuits, IEEE Trans. Appl. Super cond., vol. 21, no. 3, pp. 671–676, Jun. 2011.

[15] S. B. Kaplan et al., ―A superconductive flash digitizer with on-chip memory, IEEE Trans. Appl. Super cond., vol. 9, no. 2, pp. 3020–3025, Jun. 1999.

[16] M. Maruyama, H. Suzuki, Y. Hashimoto, and M.Hidaka,―A flash ADC using Complementarily Combined SQUIDs, IEEE Trans. Appl. Super cond., vol. 19, pp. 680–684, Jun. 2009.

[17] H. Suzukietal. ,―Design and demonstration of a 5-bit flash-type SFQADC integrated with error-correction and interleaving circuits,‖ IEEE Trans. Appl. Super cond., vol. 21, no. 3, pp. 671–676, Jun. 2011.

[18] K. Lakshmi kumar, R. Hadaway, and M. Copeland,―Characterization and modeling of mismatch in MOS transistors for precision. Analog design, IEEE J. Solid-State Circuits, vol.SSC-21, no.6, pp.1057–1066, Dec. 1986.

