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Implementation of Area optimized Flash ADC layout by using 250 nm Technology:- A Review

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Abstract— This project emphasizes on the construction of the standard cell of a 4 bit ADC using 250 nm Standard CMOS implementation process. The project highlights the complete layout of the standard Cell of a CMOS Analog comparator and its effective area optimization to obtain high degree of modularity in cell based designs. The project also focuses on implementing a Digital standard Cell Library which is further used down road to construct the 16:4 priority encoder. The Layout is extracted using 250 nm standard process to obtain the equivalent SPICE netlist. The layout is later simulated for all test vectors. Analog to Digital Converter (ADC) plays an important role in digital signal processing systems. The main challenges of designing ADC for system on chip applications are high speed, low voltage, and low power consumption. Reducing the power consumption is a major concern in a portable device. Low power techniques are applied to prolong the battery life of a system. Similarly ADCs also require a low power technique in the design to reduce the total power consumption of ADC. Speed, power dissipation and resolution are the three crucial parameters the design of any ADC which cannot be changed once the design is complete. In wireless and mobile communication applications require a high speed ADC with low resolution. In these applications, flash ADC is the most suitable ADC because of its parallel operation. The complete conversion is done in a single cycle with the helpof a large number of comparators.

I. INTRODUCTION

Signal processing is very important in many of the system on-a-chip applications. With the advancement in technology, digital signal processing has gained significant importance in the field of telecommunication, biomedical, control systems and so on. This has necessitated the need for design of high precision data converters thereby attracting immense research in this field. Analog to digital converters (ADCs) is a mixed signal device that converts analog signals which are real world signals to digital signals for processing the information. In the recent years, the need to design a low voltage, low power, high speed and wide bandwidth analog-to-digital converter has increased tremendously. Therefore the focus of this research is to design efficient low voltage ADCs that operate at high speed. Feature size of transistor is now approaching 100 nanometer in semiconductor technology and very soon it will be less than 100 nanometer and because of this trend of technology there are some challenges in the circuit designing of analog-digital mixed signal devices. To manufacture a system on chip there must be a mixed signal circuitry integrated on a single chip with memory and logic circuits. And this whole system of mixed signal circuitry along with memory & logic circuits must operates at fast speed otherwise it could become a major bottleneck to the whole system. Since the ADC is one of the IC in the mixed signal family, it has to follow this complete system on chip trend. Further this chapter will introduce the challenges in the ADC designing & some solid state technologies for complete system on chip.

A. Challenges in Designing of ADC's for System on Chip

There are many challenges for an ADC to be suitable for current System on chip implementation with present mixed signal technology. The main considerations in designing and ADC are high speed, low voltage and low power. In terms of high speed [3], presently 0.130µm CMOS technology allows processor speed in excess of 2.4 GHz. However an ADC fabricated with BiCMOS process has sampling speed of 200 mega samples per second. Our next challenge is low power consumption. In the vast market of portable devices the major consideration is power consumption reduction. For portable devices ADC must follow the system on chip trend i.e. it should be integrated on a single chip along with digital devices. All devices

powered by battery are now being designed to reduce power consumption by including some power reduction techniques. In the mixed signal ICs low voltage performance is one of the difficult challenges faced by a mixed-signal circuit designer. This difficulty arises due to the relatively high threshold voltage of transistors at low operating voltage.

B. Technologies

The speed of an ADC is affected by the type of technology used to implement a converter. There are three different types of solid state technologies that are used to implement high speed ADCs: CMOS technology, bipolar technology & Gallium Arsenide (GaAs) technology. The fastest technology of the three is GaAs technology [4] and the slowest is the CMOS technology. The fastest flash ADC is implemented by using the GaAs technology. But the present GaAs technology is not compatible with the CMOs technology which makes it very difficult to use in the implementation of system on chip. On the other hand bipolar technology provides faster operation and also compatible with CMOs technology but bipolar technology requires more steps for processing and it is expensive too as compared to CMOS technology. Because of all these reasons CMOS technology is the most preferred technology for the implementation of mixed-signal circuitry for system on chip products.

C. Basic ADC Concepts

Fundamentally analog to digital conversion involves sampling the analog signal and processing the sampled signal to generate the digital output bits. The rate at which the input signal is converted to its digital form determines the conversion speed and the number of output bits represents the resolution of the ADC. Some of the basic concepts of ADC are explained below.

D. Analog to digital converter

Analog to digital converters are the basic building blocks that provide an interface between the analog world and the digital domain. As it is the main block in mixed signal applications, it becomes a bottleneck in data processing applications and limits the performance of the overall system. In this chapter we will give the introduction of a number of A/D converter architectures. We will start from the basic definition of ADC then we will look into different architecture of ADCs that include Flash, Sigma-Delta, Pipeline, Successive Approximation and Dual Slope ADCs. Vdd

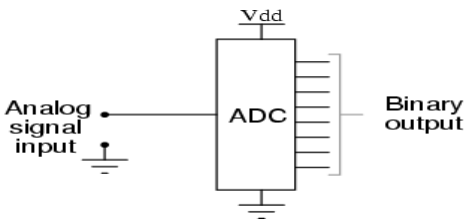

Fig. 1: Block diagram of ideal ADC

At last we will compare the different architectures and will see the impact of CMOS technology on ADC architectures.

Analog to Digital Converter (ADC) is a device that accepts an analog value (voltage/current) and converts it into digital form that can be processed by a microprocessor. Figure 1 shows a simple ADC with two inputs and 8 output bits. The signal that we want to convert into digital form is applied to input while the reference voltage should be applied to VREF. The 8 bits at the output represents the input signal in digital form.

E. ADC Architecture

An analog-to-digital converter (ADC, A/D,A to D) is a device that converts a continuous physical quantity (usually voltage) to a digital number that represents the quantity's amplitude.As all processing of signals is shifting towards digital domain (DSP) due to reduced complexity of design cycle, the high speed analog to digital and digital to analog converters are becoming important. These data converters work as interfaces between real word and the digital system. For higher speed of the complete system the ADC and DAC used should be fast. Among different architectures of ADC thee flash ADC is the fastest. Some radar systems commonly use analog-to-digital converters to convert signal strengthto digital values for subsequent signal processing. Many other in situ and remote sensing systems commonly use analogous technology

II. LITERATURE REVIEW

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[4] Hayun Chung, Alexander Rylyakov, ZeynepToprakDeniz, John Bulzacchelli, Gu-Yeon Wei, Daniel Friedman "A 7.5-GS/s 3.8-ENOB 52-mW flash ADC with clock duty cycle control in 65nm CMOS" Browse Conference Publications, 2009[4], A 7.5-GS/s 4.5-bit analog-to-digital converter (ADC) in 65nm CMOS is presented. A two-stage track-and-hold (TAH) with clock duty cycle control reduces bandwidth requirements on the slow TAH output to enable high sampling rates with low power consumption. The 7.5-GS/s flash ADC consumes 52-mW and occupies 0.01-mm2. Clock duty cycle control improves ENOB from 3.5 to 3.8 with an input sinusoid at the Nyquist frequency.

[5] Y.-S. Shu "A 6b 3GS/s 11mW Fully Dynamic Flash ADC in 40nm CMOS with Reduced Number of Comparators" VLSI Circuits (VLSIC), 2012[5]**Symposium,** A 6b 3GS/s fully dynamic flash ADC is fabricated in 40nm CMOS and occupies 0.021mm2. Dynamic comparators with digitally controlled built-in offset are realized with imbalanced tails. Half of the comparators are substituted with simple SR latches. The ADC achieves SNDRs of 36.2dB and 33.1dB at DC and Nyquist, respectively, while consuming 11mW from a 1.1V supply.

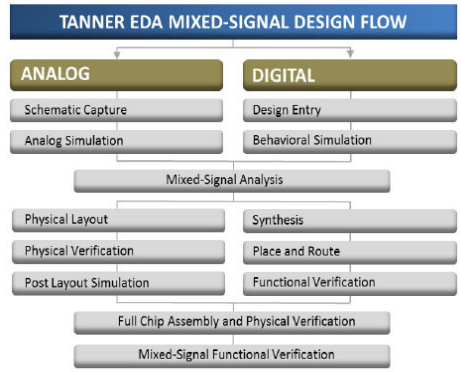
[6] V.H.-C. Chen and L. Pileggi "An 8.5mW 5GS/s 6b Flash ADC with Dynamic Offset Calibration in 32nm CMOS SOI" VLSI Circuits (VLSIC), 2013[6] Symposium, This paper describes a 5GS/s 6bit flash ADC fabricated in a 32nm CMOS SOI. The randomness of process mismatch is exploited to compensate for dynamic offset errors of comparators that occur during high speed operation. Utilizing the proposed calibration, comparators are designed with near-minimum size transistors and built-in reference levels. The ADC achieves an SNDR of 30.9dB at Nyquist and consumes 8.5mW withFoM of 59.4fJ/conv-step.

[7] R. Komar, M. Bhat, and T. Laxminidhi, "A 0.5 V 300µW 50MS/s 180nm6bit Flash ADC using inverter based comparators," in 2012 International Conference on Advances in Engineering, Science and Management(ICAESM). IEEE, 2012, This paper presents an ultralow power 6 bit Flash ADC designed in 180 nm CMOS technology for ultralow power applications. The design uses inverter based comparators to reduce the silicon area and power requirement. A novel clock delaying technique is used to power on the three stages of the comparator which work in series. This reduces the power consumption and increases speed of operation. Fat tree architecture is used to design the digital encoder. The power supply used for the design is 0.5 V and the sampling rate is 50 MS/s. The design consumes ultralow power of 600 µW and spans a very small area of 0.164 mm2. In literature this is found to be the lowest for 6 bit ADCs in 180 nm with sampling frequency of 5 MS/s or above. The SNDR remains above 31.5 dB in the whole input frequency range of 0 to 25 MHz. The ADC has maximum DNL of 0.85 LSB and maximum INL of 1 LSB. The FOM of the ADC is found to be 0.39 pJ/conv.

III. PROPOSED METHODOLOGY

A.Proposed Design Method Tanner Eda software:

Tanner EDA tools for analog and mixed-signal ICs and MEMS design offers designers a seamless, efficient path from design capture through verification. Our powerful, robust tool suite is ideal for applications including Power Management, Life Sciences / Biomedical, Displays, Image Sensors, Automotive, Aerospace, RF, Photovoltaics, Consumer Electronics and MEMS. In this we use S-Edit, T-Edit and W-Edit.



B. Introduction

Micro wind:

The MICROWIND software allows the designer to simulate and design an integrated circuit at physical description level. Born in Toulouse (France), Micro wind is an innovative CMOS design tool for educational market.

Micro wind is developed as comprehensive package on windows platform to enable students to learn smart design methods and techniques with more practice. With inbuilt layout editing tools, mix-signal simulator, MOS characteristic viewer and more, it allows students to learn complete design process with ease.

Micro wind unifies schematic entry, pattern based simulator, SPICE extraction of schematic, Verilog extractor, layout compilation, on layout mix-signal circuit simulation, cross sectional & 3D viewer, netlist extraction, BSIM4 tutorial on MOS devices and sign-off correlation to deliver unmatched design performance and productivity.

With its approach for CMOS design education, Micro wind has gained lot followers worldwide. Universities across the globe are using Micro wind for budding engineers to teach CMOS concepts with ease. Paving their path for more skilled softwares to be used at later stage of their course work.

IV. DESIGN MODULES

Flash analog-to-digital converters are the fastest ADCs among the other types of AD converters. It can achieve extremely high speed with low resolution. In real world, signal such as voice, image and other information are analog, but in electronics device, only digital signal can be processed, which means all analog signals needs to be converted into digital signal. An ADC is supposed to complete such conversions. It converts the analog signals

(voltages, current and etc.) into digital signal (normally binary), which will be processed by a DSP in electronic device. On the other hand, a digital-to-analog converter (DAC) Perform opposite way (DAC is not discussed in the thesis). Digital signal processed by a DSP are sent to a DAC and converted to analog to digital signals so that people can hear the music, see the image, and etc. Therefore, it obvious that the analog-to-digital converter is an indispensable part and play a key role. It is like a translator connecting the real world and the electronic device. Whatever the electronics are evolving, since the real word is analog, the AD/DA converter can never be disappeared. This may be the only motivation of researching and designing AD/DA converters. There are many different type of analog to digital converters which are used for quite distinct purpose. People design FLASH ADCs according to their specifications requirements. Among all kind of FLASH ADCs, high speed FLASH ADC is becoming more and more important and widely applied nowadays. For example, low-to-medium bit resolution very high speed (4-8 bits and over several GSps speed) ADCs have applications in UWB system, disk driver, radar detector, wide band radio receiver and optical communication links, while medium-to-high bit resolution high speed ADCs (8-14 bits and hundreds of MSps to 1-2 GSps speed) have application in CCD imaging, ultrasonic medium imaging, digital receivers, base station, digital video, cable modems and fast Ethernet.

A. Architectural Details

Flash ADCs are made by cascading high-speed comparators. A 3-bit flash converter shown in **Figure 1**flash ADC block diagram. For an N-bit converter, the total number of flash or parallel comparators 2N-1. In this ADC ,2Nresistors and 1-priority encoder type (2N*n) are needed. A resistive-divider with 2N resistors provides the reference voltage. The reference voltage for each comparator is one least significant bit (LSB) greater than the reference voltage for the comparator immediately below it. Comparator produces a 1 when its analog input voltage is higher than the reference voltage applied to it. Otherwise, the comparator output is 0.

B. Operation

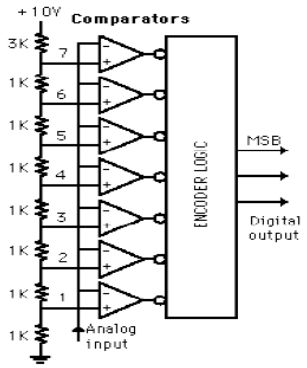


Fig 3: 3-bit flash converter.

As thetruth table in fig 3, it is clear that 1-pariority encoder gives the output as digital form. With VA<1V, all the comparators outputC1 toC7 will be high. With VA>1V, one or more of the comparator output will be LOW. The comparator outputs are fed into active-LOW priority encoder that generates a binary output corresponding to the highest numbered comparator output that is LOW. For example, when VA =3.5V, outputs C1 ,C2and C3 will be LOW and all others will be HIGH.

V. CONCLUSION AND FUTURE SCOPE

Conclusion: - A new dynamic ADC which shows lower power consumption and high speed than the conventional dynamic latched ADCs has been designed. With two additional inverters inserted between the input- and output-stage of the conventional double tail dynamic ADC, the gain preceding the regenerative latch stage was improved and the complementary version of the output-latch stage, which has bigger output drive current capability at the same area, was implemented. Because ADCs have only two output states, their outputs are near zero or near the supply voltage. Here, clocking technique has been used to switch faster at intermediate nodes and reduces the power dissipation. So, a PMOS used between nodes. When clock is zero, then both nodes should be at same potential (by shorted the nodes using PMOS at clock=0). Here, the W/L ratios also arranged of each transistor to reduce the power consumption in the ADC. This process is carried out at 5GHz clock frequency and 180nm technology.

It is known that ADC is mainly used in ADCs and relaxation oscillators. But it should be low power consummator during active operation and in sub-threshold condition. . It also reduces kickback noise so that kickback noise should not affect intermediate voltage or current. In previous design, researcher did not give method to calculate kickback noise. So kickback noise has been calculated in new circuit with the help of a resistor and capacitor (connected at the input terminals InN and InP). As synchronous systems are running faster and faster, clocked ADCs must run at a higher speed, as well. A common clocked architecture that can achieve a high rate of operation has two phases of operation: evaluation phase and reset phase. A ADC consists of a specialized high-gain differential amplifier. They are commonly used in devices that measure and digitize analog signals, such as analog-to-digital converters. By only stroking a ADC at certain intervals, higher accuracy and lower power can be achieved with a clocked (or dynamic) ADC structure.

Future Work:- As mentioned earlier, since the proposed fully dynamic latched ADC can be optimized for either the minimum kickback noise voltage or the maximum load drivability at a limited area according to the design specification, searching for the most suitable application can be one topic for the future works. In addition, kickback noise cancellation techniques can be considered for further reduction of the kickback noise voltage.

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