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Design and Implementation of Area Efficient Three Input XOR/XNOR Gate for Low Power CMOS Logic Design using Micro wind:- A Review

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Abstract— This thesis work addressed new low power approaches for Very Large Scale Integration (VLSI) logic and memory. Power dissipation is one of the major concerns when designing a VLSI system. Until recently, dynamic power was the only concern. However, as the technology feature size shrinks, static power, which was negligible before, becomes an issue as important as dynamic power. Since static power increases dramatically (indeed, even exponentially) in nano scale silicon VLSI technology, the importance of reducing leakage power consumption cannot be overstressed. A well known previous techniques cut off Vdd and/or Gnd connections of transistors to save leakage power consumption. However, when transistors are allowed to float, a system may have to wait a long time to reliably restore lost state and thus may experience seriously degraded performance. Therefore, retaining state is crucial for a system that requires fast response even while in an inactive state. Our thesis provides new VLSI techniques that achieve low leakage power consumption while maintaining logic state, and thus can be used for a system with long inactive times but a fast response ime requirement. Contribution of this work, we proposed a Power and area efficient of Three Input XOR/XNOR Gate Using CMOS Logic Design. The newly design Three Input XOR/XNOR circuit takes less power. All proposed circuit design and power reduction approach were implemented in HSIPCE and tested on different Three Input XOR/XNOR circuits.

Keywords— CMOS, XOR, NAND, NOR, MICROWIND

I. INTRODUCTION

XOR XNOR gate is a fundamental operating unit in computing and it is used as a basic cell to implement a VLSI model circuit in many processing applications such as multiplier, digital filter, CPU, etc. Therefore many concepts of Three input OR/XNOR have been studied in order to reduce the power consumption. A world without electronics cannot be imagined in the present generation. The use of electronic items has encompassed our regular work day to such a degree that it is impracticable to spend a few hours without them. At the outset of the day to its end, we use a brigade of electronic gadgets to enhance various problems solving performance. In sum, we are very dependent on the electronics, as they facilitate our day to day routine. For example, the use of mobile phones has changed the definition of communication. The Smartphone was introduced to the public in 1993, with added description like: gaming, email, etc. Instead of physical buttons, the users touch the screen to select the required options. Researchers found that its usage has had a rapid increase from the year 2006 till present. According to recent survey, 77 percent of the world population uses the mobile phone. Also we use a variety of portable electronic devices which are inbuilt with a variety of operating systems. It is not easy for us to imagine the world without electronic devices.

Digital Signal Processing (DSP) is commonly used in devices such as mobile phones, laptops, multimedia computers, camcorders, CD players, hard drives etc. A DSP chip is a programmable device, which has a set of instructions that enable various algorithms to be coded into it. The adder is one of the key components of a DSP chip. Current devices like microprocessors have become quite powerful with the ability to perform millions of operations per second. As the number of transistors on a chip increases, the power consumption becomes a concern especially for use in portable electronics. Power consumption is one of the top concerns of Very Large Scale Integration (VLSI) circuit design, for which Complementary Metal Oxide

1.2 Exclusive-Or (XOR) and xnor The fundamental Exclusive-OR (XOR) and Exceptional-NOR (XNOR) gates are of a couple of computerized strategies and are massively utilized as a part of extremely colossal scale

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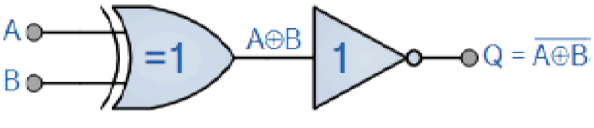
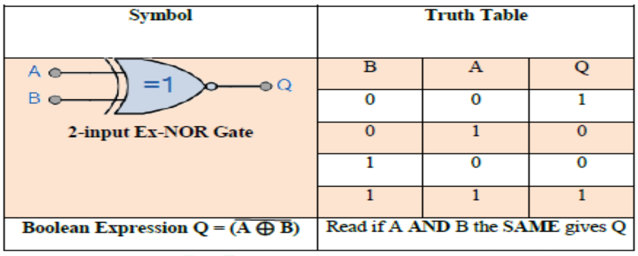
coordination methods reminiscent of equality checkers, comparators, crypto processors arithmetic and common sense circuit experiment sample mills, especially in Three input XOR/XNOR module as Sum output that is 3-input XOR and many others. In these sorts of projects, XOR and XNOR gats constitute part of the important course of the framework, which significantly influences the most pessimistic scenario stretch and the general execution of the method. An enhanced plan is liked to turn away any corruption on the yield voltage, expend less power, and have substantially less delay in imperative course with sub-micron innovation we profound to scale down low-supply. In our approach, we recognize a fundamental cell phone together with three-input and two outputs. Consequent and if fundamental we rehearse a considerable amount of redress components and enhancement techniques to get adjusted 3-input XOR–XNOR circuits.



2-input "Ex-OR" gate plus a "NOT" gate

Fig.1 2-Input XOR Gate

Table 1.1 2-input Ex-NOR Gate



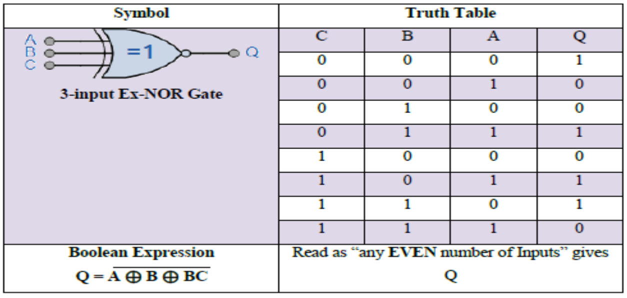
Symbol	Truth Table		
2-input Ex-NOR Gate	B	A	Q
	0	0	1
	0	1	0
	1	0	0
	1	1	1
Boolean Expression $Q = (\overline{A \oplus B})$	Read if A AND B the SAME gives Q		

Then an Ex-NOR function with more than two inputs is called an "even function" or modulo-2-sum (Mod-2-SUM), not an Ex-NOR. This description can be expanded to apply to any number of individual inputs as shown below for a 3-input Exclusive- NOR gate.

3-input Ex-NOR Gate

Giving the Boolean expression of: Q = ABC' + AB'C + A'BC + ABC We said previously that the Ex-NOR function is a combination of different basic logic gates Ex-OR and a NOT gate, and by using the 2-input truth table above, we can expand the Ex-NOR function to: Q = (A ⊕ B) = A'B + AB' which means we can realize this new expression using the following individual gates

Table 1.2 3-input Ex-NOR Gate



Symbol	Truth Table			
3-input Ex-NOR Gate	C	B	A	Q
	0	0	0	1
	0	0	1	0
	0	1	0	0
	0	1	1	1
	1	0	0	0
	1	0	1	1
	1	1	0	1
	1	1	1	0
Boolean Expression $Q = \overline{A \oplus B \oplus BC}$	Read as "any EVEN number of Inputs" gives Q			

Static logic is a design methodology in integrated circuit design where there is at all times some mechanism to drive the output either high or low. For example, in many of the popular logic families, such as TTL and traditional CMOS, there is always a low-impedance path between the output and either the supply voltage or the ground. The most widely used logic style is static CMOS. A static CMOS gate is a combination of two networks, called the pull-up network (PUN) and the pull-down network (PDN). The function of the PUN is to provide a connection between the output and VDD anytime the output of the logic gate is meant to be 1(based on the inputs). Similarly, the function of the PDN is to connect the output to VSS when the output of the logic gate is meant to be 0 (based on the inputs). The PUN and PDN networks are constructed in a mutually exclusive fashion such that, one and only one of these networks is conducting in the steady state. Dynamic logic is a design methodology in integrated circuit design in that it uses a clock signal in its implementation of combinational logic circuits. In dynamic logic, there is not always a mechanism driving the output high or low. In the most common version of this concept, the output is driven high or low during distinct parts of the clock cycle. Dynamic logic requires a minimum clock rate fast enough that the output state of each dynamic gate is used before it leaks out of the capacitance holding that state. The basic construction of a dynamic logic gate is shown in fig.2. The PDN (pull-down network) is constructed exactly as in complementary CMOS. The operation of this circuit is divided into two major phases: precharge and evaluation, with the mode of operation determined by the clock signal CLK

II. LITERATURE REVIEW

Tooraj Nikoubin et al.,(2016), We observed that a, SCDM serves as a design methodology for three-input XOR/ XNOR, which is one of the most complex and competitive as well as all-purpose three-input basic gates in arithmetic circuits. In the end, three new high performance three-input XOR/XNOR circuits with less PDP and occupied area are conceived using SCDM. The new circuits enjoy higher driving capability, transistor density, noise immunity with low-voltage operation, and the least probability to produce glitches. As a unique feature, the critical path of the presented designs consists of only two transistors, which causes low propagation delay.

Gopal et. al (2016), in these project two novel design methodologies of low voltage OR-XNOR circuits are tested. The performances of the proposed circuits can operate at low-voltages, and have good output levels. The proposed circuits tested to have noise immunity, higher energy-efficiency and faster operation. In the end, new high-performance three-input XOR-XNOR circuits with less PDP and occupied area are designed.

Tung et. al (2013), this paper proposes a low-power, high speed full adder (FA), abbreviated as LPHS-FA, is presented as an elegant way to reduce circuit complexity and improve the performance thereof. Employing as few as 15 MOSFETs in total, an LPHS-FA requires 60-73% fewer transistors than other existing FAs with drivability. For validation purpose, HSPICE simulations are conducted on all the proposed and referenced FAs based on the TSMC 0.18-? m CMOS process technology. The LPHSFA is found to provide a 20.4-21.2% power saving, a 12.3-67.0% delay time reduction and a 35-102% reduction in power delay product compared with the referenced FAs. In short, an LPHS-FA is presented in a concise form as a high per formance FA in practical applications.

Y Jagadeeshet. et. al (2013), In this paper we observe that CMOS technology achieving high performance has resulted in increase of leakage power dissipation. It proposed an efficient methodology for reducing leakage power in VLSI design. Our Dual sleep approach shows improved results in terms of static power, dynamic power and power delay product. It gives the CMOS circuit designers another option in designing integrated Circuits more efficiently.

Reddy et. al (2013), This proposed work illustrates the design of the low-power less transistor full adder designs using cadence tool and virtuoso platform, the entire simulations have been done on 180nm single n-well CMOS bulk technology, in virtuoso platform of cadence tool with the supply voltage 1.8V and frequency of 100MHz. These circuits consume less power with maximum (6T design) of 93.1% power saving compare to conventional 28T design and 80.2% power saving compare to SERF design without much delay degradation. The proposed circuits exploit the advantage of GDI technique and pass transistor logic.

Md. Asif et. al (2012), and in this paper we observe that CMOS technology achieving high performance and it uses the methodology for reducing leakage power in VLSI design. Variable Body Biasing approach shows improved results in terms of static power, dynamic power and power delay product. It gives the CMOS circuit designers another option in designing integrated circuits more efficiently

III. METHODOLOGY

A. Transient Power Consumption Transient power consumption is due to the current that flows only when the transistors of the devices are switching from one logic state to another and this is result of the current required to charge the internal nodes (switching current) plus the through current (current that flows from VCC to GND when the p-channel transistor And n-channel transistor turn on briefly at the same time during the logic transition).The frequency at which the device is switching, and the rise and fall times of the input signal, as well as the internal nodes (points) of the device, has a direct effect on the duration of the current spike. For fast input transition rates, the through current of the gate is negligible compared to the switching current. For this reason, the dynamic supply current is governed by the internal capacitance of the IC and the charge and discharge current of the load capacitance.
Transient power consumption is calculated using equation 4.

$$PT = Cpd \times Vcc\ 2 \times FI \times NSW \text{ ....(4)}$$

Where:
PT = transient power consumption
VCC= supply voltage
FI = input signal frequency
NSW = number of bits switching
Cod= dynamic power-dissipation capacitance
In the case of single-bit switching, NSW in equation 4 is 1.
Dynamic supply current is dominant in CMOS circuits because most of the power is consumed in moving charges in the parasitic capacitor in the CMOS gates. As a result, the simplified model of a CMOS circuit consisting of several gates can be viewed as one large capacitor that is charged and discharged between the power supply rails. Therefore, the power–dissipation capacitance (Cpd) is often specified as a measure of this equivalent capacitance and is used to approximate the dynamic power consumption. Cod is defined as the internal equivalent capacitance of a device calculated by measuring operating current without load capacitance. Depending on the output switching capability, Cod can be measured with no output switching (output disabled) or with any of the outputs switching (output enabled). Cpd is discussed in greater detail in the next section.

B. Layout Design Layer Representations With increase of complexity in the CMOS processes, the visualization of all the mask levels that are used in the actual fabrication process becomes inhibited. The layer concept translates these masks to a set of conceptual layout levels that are easier to visualize by the circuit designer. From the designer’s viewpoint, all CMOS designs have the following entities:

- Two different substrates and/or wells: which is p-type for NMOS and n-type for PMOS?
- Diffusion regions (p+ and n+): which defines the area where transistors can be formed. These regions are also called active areas. Diffusion of an inverse type is needed to implement contacts to the well or to substrate. These are called select regions.
- Transistor gate electrodes: Poly silicon layer
- Metal interconnect layers
- Interlayer contacts and via layers.
- The layers for typical CMOS processes are represented in various figures in terms of:
- A color scheme (Mead-Conway colors).

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- Other color schemes designed to differentiate CMOS structures.
- Varying stipple patterns.
- Varying line styles.

An example of layer representations for CMOS inverter using above design rules is shown below Figure. Poly silicon crosses diffusion, transistors are created and where metal wires join diffusion or poly silicon, contacts are formed. This notation indicates only the relative positioning of the various design components. The absolute coordinates of these elements are determined automatically by the editor using a compactor. The compactor translates the design rules into a set of constraints on the component positions, and solves a constrained optimization problem that attempts to minimize the area or cost function.

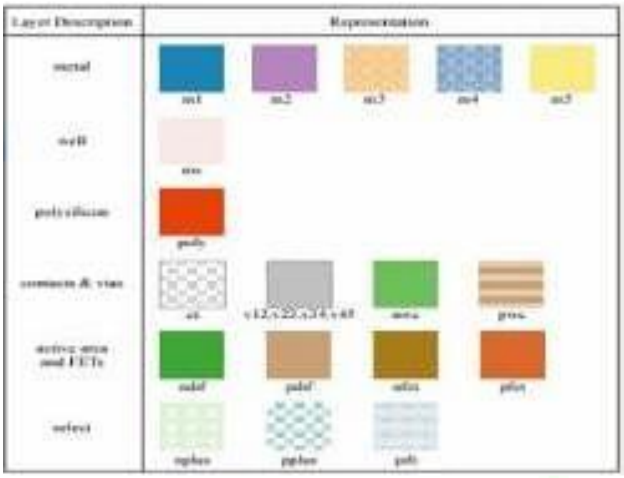

Fig 3 (a). Mead Conway Color coding for layers. [5]

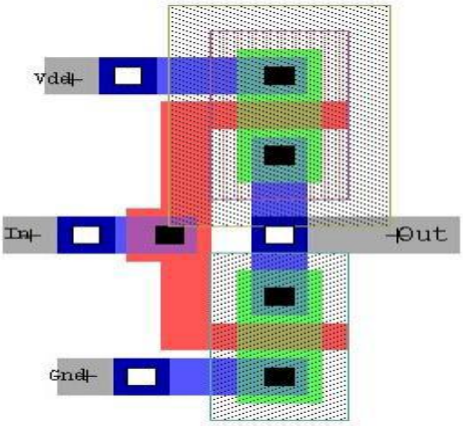

Fig.3(b) CMOS Inverter Layout Figure [5]

final layout is physically correct. The disadvantage of the symbolic approach is that the outcome of the compaction phase is often unpredictable. The resulting layout can be less dense than what is obtained with the manual approach. In addition, it does not Show exact placement, transistor sizes, wire lengths, wire widths, tub boundaries. For example, stick diagram for CMOS Inverter is shown below.

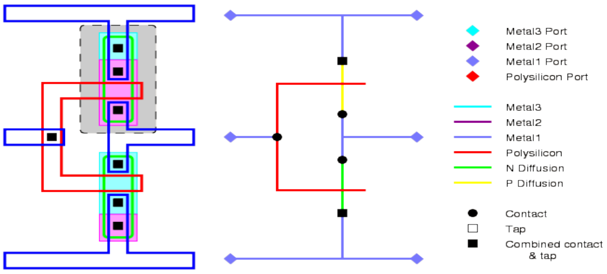

Fig.4 Stick Diagram of a CMOS Inverter [5]

IV. CONCLUSION AND FUTURE SCOPE

In nanometer scale CMOS technology, sub threshold leakage power is compatible to dynamic power consumption, and thus handling leakage power is a great challenge. In this dissertation, a new circuit design named “Low Power and area efficient of Three Input XOR/XNOR Gate Using CMOS Logic Design” to tackle the leakage problem will be discussed.

In this dissertation, a static power reduction technique named “Dual Sleep” is proposed. This technique enables us to reduce the static power consumption in low power CMOS circuit without penalizing in delay or area. This design technique offers the low power CMOS circuit designer’s new armour in their arsenal. A Three Input XOR/XNOR circuit called Low-Power Three Input XOR/XNOR. Our Low-Power Three Input XOR/XNOR provides a new way to save power consumption of a circuit. After designing of Three Input XOR/XNOR is proposed. Here, a heavily researched area: low-power VLSI design For systems spending a large percentage of time in Previous work, typically resulting in approximately two orders of magnitude less leakage power over the best of all prior known state-saving VLSI design approaches is being explored.

- We have implemented our design in chain of four inverters, 1 bit full subs tractor and SRAM circuit. More tests could be done on ISCAS benchmark\ circuits for further verification.
- In our design we tried to keep the area equal to previous cases. Further research could be done to explore design techniques to reduce delay and areas well as static power, hence overall increase of circuit performance.
- The proposed circuit is used in ALU to improve the performance. And optimized power dissipation.
- The proposed circuit is used in digital signal processing (DSP) and microprocessor to improve the performance.

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