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Design and Implementation of Power Efficient 2:1 Multiplexer Design for Low Power VLSI Applications:- A Review

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Abstract— Today power dissipation has become the main design concern in VLSI circuits. As the technology advances, the number of transistors integrated on a single chip increases and the switching speed of the transistors also increases. More expensive packaging and cooling techniques are required for high performance systems because of more heat dissipation and it also degrades the system reliability. In this paper, a new technique based on adiabatic logic will be presented for reducing the power dissipation which shows an increasing growth as the technology is scaled down. Using adiabatic technique, power dissipation in transistors can be minimized as well as the energy stored on the load capacitance can be reused instead of dissipated as heat. In this paper, we have proposed a2:1 multiplexer using ECRL, PFAL & DFAL adiabatic logic design techniques and then compared with the conventional CMOS multiplexer. A multiplexer is an integral part of the any digital circuit and is used in variety of applications e.g. in Full Adders, Shift registers, Arithmetic Logic Unit (ALU), Digital Compressor etc. Tanner 14.1 EDA tool is used for the simulation & verification of the circuit with 90nm CMOS Technology. Due to growing market of portable electronic devices such as cell phones, personal digital assistants, laptopsetc, low power consumption has become a major concern in integrated circuit design.

Keywords— Multiplex, Power dissipation, Feedback, CMOS, NAND, NOR

I. INTRODUCTION

In applied physics, an adiabatic process is defined as any process that is asymptotically isentropic (thermo-dynamically reversible), that is, whose total entropy generated tends towards zero in some appropriate limit (typically, of low speed and/or improved isolation of the system). As the most famous example, asymptotically Reversible heat engines were first described by Carnot in 1825, and were shown by him to provide the maximum possible thermodynamic efficiency. Part of the cycle of Carnot's engines involved processes with no heat flow, and this lack was the original and literal meaning of the term adiabatic. But today, we would call the entire Carnot cycle adiabatic, in the more general applied-physics sense of the term, which has departed from the literal meaning. Of course, no real physical process can be arranged to be absolutely perfectly isentropic (with entropy generated being exactly zero) since there will always be some nonzero base rate of unwanted dissipative interactions with the environment (e.g., quantum tunneling, cosmic rays, asteroid impact). However, in practice, if the goal is to minimize the energy dissipation of some process, much can be done to bring the expected dissipation of the process as close to zero as is possible, within the constraints of the available technology. We use the term adiabatic to refer to the general engineering study of ways to minimize the entropy generation of real physical processes. The field of adiabatic circuits applies the general concepts of adiabatic to the design of low-power electronic circuits in particular, consisting primarily today of digital MOSFET-based switching circuits.

II. LITERATURE REVIEW

Yazdi Ahmad, et. al. investigates the output waveforms of various2:1 multiplexer (2:1 MUX) circuits in different CMOS (Complementary MOS) logic styles at deep sub threshold/ low-frequency region at 16-nm technology node. It further compares the average power dissipation (taking both dynamic and leakage power into consideration) of those 2:1 MUX circuits which offer reliable output waveform to find out the best CMOS logic style for ultra low power applications. Authors successfully investigated different CMOS based 2:1 MUX circuits to find the best design in terms of average power dissipation in deep-sub threshold/low frequency region at supply voltages ranging from 130 mV – 150 mV for ultralow-power applications. Transmission gate based design (CMOSTG) exhibits

acceptable output levels and dissipates least average power compared to other CMOS logic styles. The proposed CNFET (TG) based 2:1 MUX further improves other design matrices compared to its CMOS counterpart and hence can be an attractive choice to replace MOSFET version of 2:1 MUX circuit [1].

Ahmed M. Shams, et. al. puts forward a methodology for designing 1 bit full adder using a 2T mux. The 2T mux is combined in a specific manner to get a full adder with sum and carry output. The resulting 1 bit full adder is made up of 16 transistors. The simulation is done using Cadence Virtuoso Simulator using 180nm technology and 1.8V power supply. The results show the efficiency of the design, the full adder designed using this 2T mux is found to be efficient from both speed and power perspective. Reduced number of transistors also helped in reducing the power dissipation and increasing the speed of the design. [2].

Hing Mo Lam, et. al. Represent the simulation of different 2:1 its comparative analysis on different parameter such as power supply voltage, operating multiplexer is known as mux. It is a device that helps in selection a number of input signals, frequency temperature and area efficiency and its applications in 1bit full adder cell all the simulation have been followed on cadence tool at 180nm technology at virtuoso. For low-leakage and high-speed circuit concern should be on both the factor speed and power this paper concluded with the efficient approach of multiplexer at 180nm technology. Modified differential cascade voltage switch logic(MDCVSL) shows least power consumption over a range of power supply voltage, power-delay product, operating frequency, output load capacitance and operating temperature over other circuit design of 2:1 multiplexer. [3].

W. Athas, et. al. state that, Adiabatic switching techniques based on energy recovery principle are one of the innovative solutions at circuit and logic level to achieve reduction in power. Many researchers had taken adder as a benchmark circuit but advantage of adiabatic can be taken only for a large digital circuit. Barrel Shifter is an important block in the processor design and not much effort has been done to minimize it‘s power dissipation. A barrel shifter needs nlog2n MUX for n-bit shifting and therefore designing a MUX for low power to use it as a repetitive block in the barrel shifter will considerably reduce the simulation time. This paper compares conventional CMOS based design with adiabatic All the circuits are designed using cell based design approach and 180nm device size in Cadence. The outcome of this research work will provide guidelines for designing barrel shifter using ultra low power MUX . With the energy-recovery adiabatic switching, the circuit energies are conserved within the system rather than dissipated as heat. Depending upon the system requirements and application, this approach may be used to design ultra low power under certain conditions. These conditions are obviously defined by frequency constraints, device sizes, and silicon area overhead. Barrel shifter design can be optimized for low power, low delay and area using the results published here [4].

Simran Kaur ,et .al. focus on the dynamic power dissipation during the Write operation in CMOS SRAM cell. The charging and discharging of bit lines consume more power during the Write operation. 8T SRAM cell includes two more trail transistors in the pull down path for proper charging and discharging the bit lines. The results of 8T SRAM cell are taken on different frequencies at power supply of 1.5 V. The circuit is characterized by using the 130 nm technology which is having supply voltage of 1.5 V. Finally the results are compared with Conventional 6T SRAM cell. The power dissipated in low power 8T SRAM cell is reduced in comparison to conventional 6T SRAM cell. The result of the research has practical reference value for further study [5].

Y. Moon, et. al. have compared two adiabatic logic designs with conventional CMOS.A 2:1 multiplexer are implemented by these techniques and results are compared such as power dissipation, rise time, fall time. transistor count and maximum frequency. The designing of schematic and simulation of these logics done on TANNER v7.From results it is found that power consumption of PFAL logic is less as compare to ECRL and CMOS[6].

N.Anuar, et. al. Discuss, the growing market of mobile, battery powered electronic systems demands the design of microelectronic circuits with low power dissipation. More generally, as density, size, and complexity of the chips continue to increase, the difficulty in providing proper cooling might either add significant cost or limit the functionality of the computing systems that make use of those integrated circuits. In this paper a new adiabatic inverter is proposed. Here the circuit of conventional positive feedback adiabatic (PFAL) inverter has been improved. The various improvement results are analyzed in Tanner EDA tool. From the simulation results it is found that modified PFAL inverter has better performance than the normal PFAL inverter. The modified PFAL inverter has 70% less power dissipation over PFAL inverter. The delay characteristics are nearly 98% better in modified PFAL inverter [7].

G.RamaTulasi, et. al. presents an adiabatic logic family called positive feedback adiabatic logic circuits (PFAL).There is power reduction due to energy recovery in the recovery phase of the clock supply. The power

dissipation comparison with the static CMOS logic is performed. The simulation is performed on cadence virtuoso using 180nm CMOS technology. The result shows that power reduction of 50% to 70% can be achieved over static CMOS within a practical operating frequency range. Author found that the adiabatic PFAL offers significant power reduction and so better power performance over conventional static CMOS. The comprehensive simulation shows that PFAL circuit can recover 50% of the energy dissipated in conventional static CMOS logic. However the PFAL suffers from large switching time, so it is not suitable to application where the delay is critical. Thus suffer from low speed of operation and is not suitable for the application where fast switching is required [8].

III. METHODOLOGY

The three major sources of power dissipation in CMOS circuits is expressed using the equation given below:

$$P_{Total} = P_{Switching} + P_{Short\ Circuit} + P_{Leakage}$$
$$P_{Total} = \alpha V V_{DD} F_{CLK} C_{Load} + I_{SC} V_{DD} + I_{Leakage} V_{DD}$$

In equation above equations, the first term represents power dissipation due to transistor switching. V is the voltage swing, C Load is the load capacitance and FCLK is the switching frequency of the clock. The factor α is the activity factor which represents the fraction of the circuit that is switching. In most cases the voltage swing for V is almost same as the supply voltage VDD, in such cases the term V is replaced with the second term in the equation represents short-circuits power dissipation which is the power dissipation in the CMOS when both PMOS and CMOS are ON simultaneously. When both transistors are ON a current value of ISC flows from the supply voltage to the ground and it is known as short-circuit current ISC. Apart from these two terms viz. the switching power and short-circuit power, there is always present the power loss due to leakage currents. Leakage currents depend upon various fabrication technologies related factors like threshold voltage Vth, device dimensions, substrate injection etc. In previous years a major contribution to the power dissipation was due to the switching but we have managed it effectively by reducing the switching frequency.

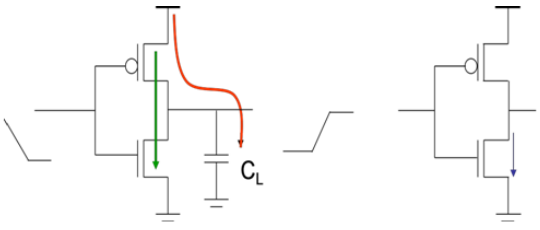

Fig.1 Power Dissipation

The Charging Process in Adiabatic Logic Compared to Static CMOS The energy dissipation due to switching of a simple CMOS inverter as shown in Fig.1 is observed. There are many ways to build a barrel shifter viz. Mux-based data reversal, Mask based data-reversal, Mask-based two's complement and Mask based One's complement. The study shows that Mux-based data reversal barrel shifter consumes less area than others and still gives better worst case delay. [5] Thus if adiabatic multiplexers are used in designing barrel shifter, the energy dissipation also can be minimized. Adiabatic techniques were used to reduce power consumption of 2:1 MUX [6]. Three adiabatic logic styles were selected Clocked CMOS Adiabatic) logic (CAL) [7], Pass Transistor Adiabatic Logic (PAL) [8] and Improved Pass Transistor Gate Logic (IPGL) [9]. The designs were made using 180nm devices and functionally simulated in Cadence tool. The simulation results were compared with that of conventional CMOS 2:1 MUX.

The fundamental concepts of adiabatic are experimentally proven with the help of adiabatic amplifier, which uses two CMOS transmission gates and two NMOS clamps. The capacitor C at the output of the gate is the input capacitance of the following gates.

Whether the PMOS or NMOS will be ON is dependent upon the input signal. If the input voltage level changes from 1 to 0, energy is transferred from the voltage source to charge the output capacitor to the supply voltage VDD. A charge of Q=CVDD is taken from the voltage source, an energy quantum of E.

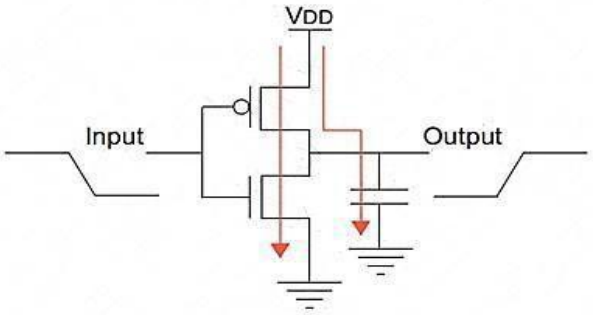

Fig. 2 Energy Dissipation

IV. CONCLUSION AND FUTURE SCOPE

The main idea of this project is to introduce the design of high-performance and power efficient full adder design using multiplexer based pass transistor logic. In the current work, the full adder design is implemented by different logics like SERF, PFAL, and ECRL etc. Further the design is implemented using pass transistor logic combined with other logic. The number of transistors required for realizing mixed CMOS design of full adder is less than the number of transistors required in realizing the design of full adder using CMOS transistors independently. So, the required logic can be realized within an optimized area which performs faster when compared to the conventional static CMOS full adder design.

Authors have implemented the 2:1 multiplexer adiabatic techniques ECRL and PFAL and compare with Conventional CMOS on 180nm technology. In this analysis, it is investigated that the PFAL has the highest level of power reduction with lowest level of power reduction at adiabatic logic level but both techniques have less power consumption as compare with CMOS. All the

parameters are computed on Multisim at 180 nm Technology at 1.5V supply voltage. A 4:1 Multiplexer can be design by adiabatic techniques for further usage in applications such as Memory Designing, in high performance low power circuits and various high end processors.

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