http://www.jctjournals.com

ISSN(ONLINE):2278 - 3814

Volume-12, Issue-09, September2023

JOURNAL OF COMPUTING TECHNOLOGIES (JCT)

International Journal

Page Number: 01-05

Design and Implementation of High Speed, Low Voltage CMOS Full Adder Circuit for Efficient Power Calculation:- A Review

[1]Saloni, [2]Dr. Arpan Dwivedi

[1] M.Tech Scholar, [2]Professor and Dean

[1, 2]SAM College of Engineering &Technology, Bhopal, M.P., India

Abstract— In today's high-speed communication world the usage of electronics portable devices is increasing day by day, as the devices are portable and compact it has to satisfy the need of low power dissipation and minimum area requirement along with the high speed. A one bit full adder cell is one of the most frequently used digital circuit component in arithmetic logic unit (ALU) and it is the essential functional unit of all computational circuit. Till now many improvement has been done in this area to refine the architecture and performance of full adder circuit design. This paper mainly focus on two novel 1-bit full adder cells which is designed on 32 nm CMOS technology with different operating frequencies at 1 v supply voltage. The GDI full adder cell requires 10 transistors, which is very less in number as compared to conventional CMOS design and the speed is also more as compared conventional CMOS design. But in other hand GDI technique suffers from voltage swing degradation due to voltage loss problem and also the major problem of a GDI full adder cell is that it requires twin-well CMOS or Silicon On Insulator (SOI) process to construct it, so it will be more expensive to implement a GDI chip. If GDI uses only standard p-well CMOS process to implement it, the new problem arises that is decrease in driving capability which makes this process more expensive and also not easy to realize.

Keywords— GDI Adder, Pass transistor, Low Power consumption, High Performance, Hybrid Logic, Transient analysis

I. INTRODUCTION

The inclination of superior and included functionalities in integrated circuit has led to forceful technology scaling throughout the years for development of semiconductor industries. As the scaling of supply voltage (VDD), threshold voltage (Vth) and the gadget geometry are required to be scaled further to meet the compatibility of low power circuits. This will prompt debased short channel impacts and increased transistor OFF-state current (IOFF) of the device with reduction of technology. Furthermore leakage power consumption, higher working frequency and on kick the bucket transistor include will prompt build add up to power consumption during scaling of technology.

Productivity of usage of arithmetic circuits in the execution of committed procedures, for example, correlation, digital filtering and convolution generally influences the execution of utilization particular coordinated circuits and advanced flag processors. The expanding density of transistors hence forth complication nature in the integrated circuits requests for rapid, power effective outlines. The specialists over the time have built up various CMOS Logic styles to meet the necessity of the quickly developing industry. Scaling down the supply voltage is a methods which results in lower power utilization of the circuit in ultra profound submicron innovation however it brings about debased driving ability and expanded circuit delay of the composed cells. The fast increment sought after of elite, convenient battery worked devices has asked for enhanced low power and rapid plans of the devices. With the clock frequencies moving toward 1GHz and that's just the beginning, the arithmetic juggling pieces must keep pace with the proceeded with interest for low power utilization.

A. *Why the Need of Low Power Designs in DSM :-*

Low energy utilization is a standout amongst the most preferred properties of present day compact electronic gadgets. On one side, the popularity of compact electronic gadgets requires the accessibility of low power modules for the outline of durable battery worked framework. On the opposite side, it requires to outline fast modules to adapt/manage current superior preparing applications. The test that has been confronted by VLSI fashioners is to discover compelling procedures and their productive application to get least power dissemination with no bargain with the other execution assessment parameters. Along these lines, the plan of low power circuits with

enhanced execution is significant worry of present day VLSI outlines. In the outline of low power circuits the choice of a legitimate rationale style assumes a critical part. The blend of certain rationale styles, low power modules with low spillage circuit topologies can incredibly diminish the disadvantages of cutting edge sub-micrometer innovations.

B. Low Power Design Requirement:-

Power Considerations: According to the formula:

$Pdyn=Vdd2.fclk.\alpha nn.cn+Vdd.iscn$

the dynamic power dissipation of a digital CMOS circuit depends on the supply voltage Vdd , the clock frequency fclk , the node switching activities αn , the node capacitances cn, the node short-circuit currents iscn , and the number of nodes n. A reduction of each of these parameters results in a reduction of dissipated power. However, clock frequency reduction is only feasible at the architecture level, whereas at the circuit level frequency fclk is usually regarded as constant in order to fulfill some given throughput requirement. All the other parameters are influenced to some degree by the logic style applied. Thus, some general logic style requirements for low-power circuit implementation can be stated at this point.

II. LITERATURE REVIEW

B.Annapoorani et. al. 2022 The adders are the vital arithmetic operation for any arithmetic operations like multiplication, subtraction, and division. Binary number additions are performed by the digital circuit known as the adder. In VLSI (Very Large Scale Integration), the full adder is a basic component as it plays a major role in designing the integrated circuits applications. To minimize the power, various adder designs are implemented and each implemented designs undergo defined drawbacks. The designed adder requires high power when the driving capability is perfect and requires low power when the delay occurred is more. To overcome such issues and to obtain better performance, a novel parallel adder is proposed. The design of adder is initiated with 1 bit and has been extended up to 32 bits so as verify its scalability. This proposed novel parallel adder is attained from the carry look-ahead adder. The merits of this suggested adder are better speed, power consumption and delay, and the capability in driving.

A. Morgenshteinet. et. al. 2002 In this paper author presented a novel technique for improvement of all the parameters which are associated with the circuit like lower power consumption this can be achieved by reducing the transistor count of the circuit therefore author has introduce a technique known as Gate Diffusion Input (GDI). The GDI technique has a huge potential to replace a conventional 28T adder circuit design in terms of area and power consumption of the circuit but circuit suffers from voltage degradation problem. This problem can be eliminated by using hybrid GDI technique. In Hybrid GDI technique, to improve output voltage level, an additional nMOS transistor can be added with basic GDI cell as shown in Figure 3.7. The nMOS transistor is added because it passes strong „0" value. The pair of additional nMOS with pMOS of GDI cell makes a single TG cell. An inverter is used activate pMOS and nMOS of TG cell simultaneously. In this design input B is applied to source of pMOS of GDI/TG cell. Now, for input values of A = 0, B = 0 and A = 0, B = 1, due to inverter before GDI cell, nMOS of GDI cell conducts and it passes strong „0" to output. When A = 1, pMOS of GDI/TG cell and nMOS of TG cell conducts simultaneously, hence input B will appear as output without any degradation .

Vijay Kumar Sharma et. al. 2020 Full adder is the heart of any central processing unit that is a core component employed in all the processors. This paper presents a design methodology for full adder circuit with minimum number of transistor i.e. reduced size & reduced area. This is then used to implement 10T full adder design for carrying out summation of bits. The analysis of the developed full adder design is done at room temperature CMOS 90 nm and 180 nm technologies using Micro wind tool 2.6.The result shows the comparison between different CMOS technologies in 90 nm and 180 nm using micro wind tool 2.6 on the design in regards of power dissipation, propagation delay and power delay product. A comparison table shown having power, delay and transistor count based comparison at 90 nm and 180 nmtechnologies showing delay in time and dissipated Power within the full adder summation circuit design at room temperatures. We will also provide the layout of the full adder design at both technologies. The proposed technique shows 96.66% less power consumption in 90 nm and 93.93% less power consumption in 180nm as compare to base paper hybrid logic design.

Adarsh Kumar Agrawalet. et. al. 2009 In this paper author presented a full adder design by using GDI technique. In Hybrid GDI based XOR gate, one more GDI cell has been added which is controlled by inverted input gate signal of first GDI cell. Both GDI cell behaves as an inverter for any different input combination of XOR gate. When A = 0, pMOS of GDI cell 1 and nMOS of GDI cell 2 conducts simultaneously. When B = 0, GDI cell 2 acts as an inverter and provides inverted input signal A at output end. It means, for B = 0, A = 0, XOR out is „1" and for B = 0, A = 1, XOR out is „0.

From the simulation, it is observed that in case of AND gate, Hybrid GDI technique does not give favorable result for low power design. It consumes 29% more power compared to CMOS and 22.8% more than PTL technique but compared to full swing GDI, it reduces 16%. But in case of OR and XOR, it consumes less power than conventional CMOS and existing GDI technique. For OR gate, Hybrid GDI technique has 27% and 43% less power than CMOS and GDI respectively. For XOR circuit, it consumes 36% and 2.8% less power than CMOS and GDI respectively.

T. Kalavathidevi et.al, 2011 In most cases, the transient analysis of a GDI cell is similar to a standard CMOS inverter. The operation of CMOS inverter is categorized into three main regions: sub-threshold region, saturation region and linear region. Eight arithmetic operations are transfer input A, increment A (A + 1), addition (A + B), addition with carry (A + B + 1), subtraction (A – B), subtraction with borrow (A – B – 1), decrement A (A – 1), and again transfer A. The four logical operations are XOR, OR, AND and NOT .

P.Kondui et. al. 2011 Shows the implementation of RAM in GDI technique and its simulation is done in 0.18µm TSMC technology with the supply voltage of 1.8V. Their result shows 16% reduction in power and 49% reduction in delay as compared with traditional CMOS technique.

R.Uma et .al. 2012 The ALU is a combinational circuit and has a regular pattern. The complete design can divide into small identical sections and connected them in cascaded through the carries. First design one section of ALU then copied it for more sections as per design requirement. For given ALU design, one section contains six inputs and two outputs. Four control signal S2, S1, S0, Cin and two inputs bits Ai and Bi are inputs of each sections and function Fi and Cout are the outputs. To design logic diagram, one method is make a truth table with 64 (= 26) entries and simply it using Karnaugh map for output functions. Another approach is to use the availability of parallel adder .

V. Foroutanet. et. al., 2014 Modify the arithmetic circuit to obtain the remaining logical operations. To generate required OR and AND function from first and third operation of , additional modification need to be done. For OR operation, change the input Ai of each full adder to Ai + Bi. Thiscan be accomplished by ORing Bi and Ai when S2S1S0 = 100. To modify equivalence operation for the generation of AND function with S2S1S0 = 110, first investigate the possibility of OR each input Ai with some Boolean function Ki. The function so obtained is then used for X. P.

Bhattacharyya et. al., 2015 presents a Multiplication is a fundamental operation in most signal processing algorithms. Multipliers have large area, long latency and consume considerable power. Therefore low-power multiplier design has been an important part in low- power VLSI system design. Digital multiplication is a series of bit shift and bit additions, where two binary numbers, the multiplier and the multiplicand are combined to calculate the product result.

N.S. Asmangerdiet. et. al. In this outline a 12 transistor floating sort adder circuit has been proposed which gives genuinely low power scattering at paces as high as 1Ghz. Power in the circuit is lessened because of the decreased exchanging movement in the circuit. The adder turns out to be a promising outline for rapid and low power circuit plan and have great execution security against high frequency . The principle downside of the circuit is the debasement of yield voltage levels because of the powerlessness of PMOS and NMOS transistors to pass 0 and 1 separately. The feeble "0" and "1" at the carry and sum separately prompt poor driving capacity.

Haseeb Pashaet et. al. 2016 Full adder circuit is a very important component in the design of application of integrated circuits in VLSI. This paper explores the design and analysis of four different 1 bit Full Adder cell using the Modified Gate Diffusion Input (MGDI) technique on optimizing the power, delay and Power Delay Product (PDP). This technique (MGDI) allows reducing power, delay and area of digital circuits, while maintaining low complexity of logic design. Through investigation is carried out for the effectiveness using combination of different low power full adder circuit design techniques. The main objective of these full adders is providing high-speed and low power consumption also provides good voltage swing. This can be achieved by applying the low power techniques for reduction of power and delay. This work presents comparison of the different low power full adder cell on the power dissipation, delay and Power delay product. The full adder design simulations are implemented using 90nm technology with Tanner EDA.

Tool. Subodh Wairyae et. al. 2011 This paper presents a comparative study of high-speed and low-voltage full adder circuits. Our approach is based on hybrid design full adder circuits combined in a single unit. A high performance adder cell using an XOR-XNOR (3T) design style is discussed. This paper also discusses a high-speed conventional full adder design combined with MOSCAP Majority function circuit in one unit to implement a hybrid full adder circuit. Moreover, it presents low-power Majority-function-based 1-bit full adders that use MOS capacitors (MOSCAP) in its structure. This technique helps in reducing power consumption, propagation delay, and area of digital circuits while maintaining low complexity of logic design. Simulation results illustrate the superiority of the designed adder circuits over the conventional CMOS, TG, and hybrid adder circuits in terms of power, delay, power delay product (PDP), and energy delay product (EDP). Post layout simulation results illustrate the superiority of the newly designed majority adder circuits against the reported conventional adder circuits. The design is implemented on UMC0.18 µm process models in Cadence Virtuoso Schematic Composer at 1.8 V single-ended supply voltage, and simulations are carried out on Specter S.

III. PROBLEM FORMULATION

The GDI method is a standout amongst the most encouraging logic outline techniques in Adder circuit design. The GDI (Gate Diffusion Input) procedure is a low power rationale plan strategy which empowers usage of an assortment of complex logical capacities utilizing only two transistors PMOS and NMOS combining all four transistors generate EXOR gate. This system is fitting for

outline of low power, fast circuits while utilizing few number of transistors (when contrasted with CMOS and other existing methods). The primary inconvenience of the GDI adder is loss of voltage swing which reduces the driving ability of the GDI Adder circuit.

The Pass Transistor Logic (PTL) likewise turns out to be an effective approach to configuration circuits planned for low power applications were minimum no of transistor is required. With the forceful scaling of the transistor estimate because of developing technology, the significance of pass transistor logic has expanded immensely; it is because of the lower hub capacitance acquired in the PTL when contrasted with the node capacitance in CMOS circuit design. The few transistors for the execution of PTL plans are gotten by quickly diminishing the channel lengths of the transistors. The few parameters which is measured help the transistors in lessening the drop (IR drop) across the circuit. Because of these qualities, PTL union turns into a reasonable rationale plan procedure for doing low power, territory effective outlines to meet the necessities of quickly developing electronic industry

IV. METHODOLOGY IN EXISTING ADDERS

Effectiveness of usage of number arithmetic circuits in the execution of committed calculations, for example, advanced sifting, connection and convolution to a great extent influences the execution of utilization particular coordinated circuits and computerized flag processors when circuit is implemented on digital platform. The expanding thickness of transistors in deep sub-micron technology, increases the transistor count according moors law which results faster operation of the circuit and control the productive plans of digital adder circuit. The scientists over the time have built up various CMOS Logic based styles to meet the prerequisite of the quickly developing industry. Different strategies according to the requirement have been proposed throughout the years for the plan of low power design for grows of semiconductor industries for higher speed with ideal region on the chip. These methods used a specific rationale styles to plan a specific circuit by taking all parameters into consideration. Every system have its own particular focal points and impediments and advancement of a adder circuit execution had been focused through different outlines by utilizing these low power plan procedures a portion of the low power circuit outline methods viz. the customary CMOS plan system, pass transistor procedure, transmission entryway strategy and GDI method, have been talked about beneath with different adder outlines in light of these strategies by reducing the technology.

V. CONCLUSION AND FUTURE SCOPE

As we discuss in previous chapters for both existing and proposed circuit it is concludes in over both proposed 13T Hybrid GDI full adder circuits shows better performance in terms of lower power consumption in DSM circuits, provides lower delay to the circuit and over all there is improvement in Power Delay Product (PDP) than all the existing full adder circuits and proposed XOR and XNOR based circuits which is free from the degradation of the voltage level problem with all the existed circuits when compared with proposed circuit. We have compared all the existing adder circuits with the proposed from the simulation results it is observed that proposed circuits has better performance than other existing adders circuit in terms of power consumption of the circuit, propagation delay of the circuit and overall PDP. In over proposed circuit which is made from XOR single bit GDI hybrid adder circuit which shows maximum saving of power 53.2 % when comparison with existing 16T hybrid adder, maximum reduction propagation delay a maximum of 93.4 % in conventional 28T CMOS adder and the maximum PDP is achieved 96.8% in comparison to conventional 28T CMOS adder while. In proposed XNOR based full adder circuits saves maximum reduction of power upto 56.7 % when compared with to the existing 16T hybrid adder circuit, reduction of delay a maximum of 93.5 % when compared with conventional 28T CMOS adder and maximum saving of PDP up to 97.1 % compared with conventional 28T CMOS adder at lower frequency range upto 100 MHz. As we scale down the technology at 65 nm, The proposed XOR based full adder cell circuits saves the power upto 85.2 % when compared to the existing SERF adder circuit, reduction in delay upto 93.4 % when compared with SERF adder and maximum saving of PDP upto 99 % in comparison to SERF adder. The XNOR based proposed single bit full adder cell circuits produce reduction in power consumption a maximum of 86.8 % in comparison to the existing SERF adder, produces reduction in delay a maximum of 93.7 % in comparison to the SERF adder and a huge reduction in PDP a maximum of 99.2 %in comparison to SERF adder at 100 MHz frequency**.**

REFERENCES

[1] A. Morgenshteinet. al. “Gate-Diffusion Input (GDI) - A Power-Efficient method for digital combinatorial circuits” IEEE Transactions on VLSI systems, vol.10, no. 5, pp.43-51, October 2002.

[2] Adarsh Kumar Agrawal, S. Wairya, R.K. Nagaria and S. Tiwari, “A New Mixed Gate Diffusion Input Full Adder Topology for High Speed Low Power Digital Circuits”, World Applied Sciences Journal, pp.138-144, 2009.

[3] T. Kalavathidevi and C. Venkatesh, “Area Efficient Low Power VLSI Architecture for A Viterbi Decoder Using Gate Diffusion Input (GDI) Logic Style”, European Journal of Scientific Research, vol.49, no.4, pp. 521-532, 2011.

[4] PrathyushaKonduri and Magesh Kannan.P , “ Low Power RAM using Gate-Diffusion-Input Technique : A Comparison with Static CMOS” , International Journal Of Advanced Engineering Sciences and Technologies, vol. 5, no. 2, pp.195 - 200 , 2011.

[5] R.Uma and P. Dhavachelvan, “Modified Gate Diffusion Input Technique: A New Technique for Enhancing Performance in Full Adder Circuits”, 2nd International Conference on Communication, Computing & Security, pp. 74-81 -2012.

[6] VahidForoutan, MohammadRezaTaheri, KeivanNavi, and ArashAziziMazreah, “Design of two Low-Power full adder

cells using GDI structure and hybrid CMOS logic style", INTEGRATION, the VLSI journal, vol. 47, pp.48–61, 2014.

[7] Partha Bhattacharyya, BijoyKundu et.al. " Performance Analysis of Low Power High Speed Hybrid 1-bit full Adder circuit" IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, Vol. 23, no. 10, pp. 2001-2008, 2015.

[8] Nabiallah Shiri Asmangerdi, Javad For ounchi, Kuresh Ghanbari,"A New 8- Transistors Floating Full-Adder Circuit",20th Iranian Conf. Electrical Engineering, (ICEE2012), May-2012.

[9] P. M. Lee, C. H. Hsu and Y. H. Hung, "Novel 10-T full adders realized by GDI structure", Proc. on Intl. Symp. On Integrated Circuits (ISIC2007), pp. 115-118, 2007.

[10] R. Uma and P. Dhavachelvan, "Modified Gate Diffusion Input Technique: A New Technique for Enhancing Performance in Full Adder Circuits", Proc. Of ICCCS, vol. 6, pp. 74-81, 2012.

