# CLOCKED LOGIC for LOW POWER VLSI DESIGN

Kuldeep sharma

*Electronics & Communication Department, Mewar University*
*Gangrar, Chittorgarh, India*
Kuldeep57sharma@gmail.com

***Abstract*** **— The main objective of this thesis is to provide new low power solutions for Very Large Scale Integration (VLSI) designers. Especially, this work focuses on the reduction of the power dissipation, which is showing an ever-increasing growth with the scaling down of the technologies.**

**The dynamic power requirement of CMOS circuits is rapidly becoming a major concern in the design of personal information systems and large computers. In this thesis work, a new CMOS logic family called ADIABATIC LOGIC, based on the adiabatic switching principle is presented. The term adiabatic comes from thermodynamics, used to describe a process in which there is no exchange of heat with the environment. The adiabatic logic structure dramatically reduces the power dissipation. The adiabatic switching technique can achieve very low power dissipation, but at the expense of circuit complexity. Adiabatic logic offers a way to reuse the energy stored in the load capacitors rather than the traditional way of discharging the load capacitors to the ground and wasting this energy.**

**This thesis work demonstrates the low power dissipation of Clocked transmission gate adiabatic logic (CTGAL) by presenting the results of designing various design/ cell units employing CTGAL circuit techniques. A family of full-custom conventional CMOS Logic and CTGAL units for example, an inverter, and a four-bit Carry look adder were designed.**

***Keywords*** **— Complementary metal oxide semiconductor field effect transistor (CMOS), Clock transmitted gate adiabatic logic (CTGAL).**

## I. INTRODUCTION

We have come a long way from the single transistor era in 1958 to the present day ULSI (Ultra Large Scale Integration) systems with more than 50 million transistors in a single chip.

The ever-growing number of transistors integrated on a chip and the increasing transistor switching speed in recent decades has enabled great performance improvement in computer systems by several orders of magnitude. Unfortunately, such phenomenal performance improvements have been accompanied by an increase in power and energy dissipation of the systems. Higher power and energy dissipation in high performance systems require more expensive packaging and cooling technologies, increase cost, and

Decrease system reliability. Nonetheless, the level of on-chip integration and clock frequency will continue to grow with increasing performance demands, and the power and energy dissipation of high-performance systems will be a critical design constraint.

For example, high-end microprocessors in 2010 are predicted to employ billions of transistors at clock rates over 30GHz to achieve TIPS (Tera Instructions per seconds) performance. With this rate, high-end microprocessor's power dissipation is projected to reach thousands of Watts. This thesis investigates one of the major sources of the power/energy dissipation and proposes and evaluates the techniques to reduce the dissipation.

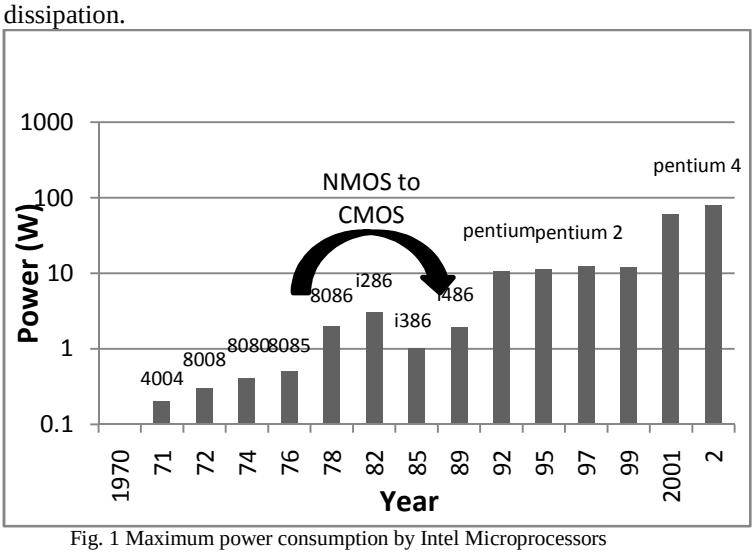



Fig. 1 Maximum power consumption by Intel Microprocessors

## II. SOURCES OF POWER CONSUMPTION IN CMOS IC

Power consumption is a primary limitation to the further advancement of semiconductor technologies. Identifying the sources of power consumption is critical for developing power reduction techniques at the fabrication technology, circuit, and architecture levels. There are mainly three sources of power consumption in CMOS circuits.

- Dynamic Power Consumption ($P_{dynamic}$)
- Leakage Power Consumption ($P_{leakage}$)
- Short-Circuit Power Consumption ($P_{short\text{-}circuit}$)

So, the total power consumption of a CMOS circuit is

$$P_{total} = P_{dynamic} + P_{leakage} + P_{short\text{-}circuit}$$

*A. Dynamic power consumption:*

The dominant component of power consumption in a typical CMOS circuit is the dynamic switching power. The dynamic switching power is dissipated while charging or discharging the parasitic capacitances during the voltage transitions of the nodes within a CMOS circuit. The dynamic switching power is independent of the type of switching gate and the shape of the input waveform (input rise and fall times). The dynamic switching power is dependent only on the supply voltage, the switching frequency, the initial and final voltages, and the equivalent capacitance of a switching node.

*B. Leakage power consumption:*

Recently, however, leakage power has become a significant portion of the total power consumption in high complexity CMOS ICs, a MOS switch has infinite input impedance. Similarly, an ideal cut-off transistor has infinite drain-to-source resistance. However, in reality, an active transistor has finite input impedance and a cut-off transistor has a finite channel resistance, producing gate oxide and sub threshold leakage current, respectively. Due to the aggressive scaling of the threshold voltages and the thickness of the gate dielectric layer in order to enhance device speed, modern MOSFETs no longer resemble, even remotely, an ideal switch. sub threshold and gate oxide leakage currents will become the dominant source of power consumption in the near future.

*C. Short – Circuit power consumption:*

In static CMOS circuits, there is a time period during the transition of the input signals when both the pull-up and pull-down network transistors are simultaneously on, thereby forming a DC current path between the power supply and ground. The DC current conducted by a CMOS circuit during an input signal transient (due to non-zero rise and fall times of the input signals) is called the short-circuit current. The short-circuit current ($I_{short\text{-}circuit}$) is temporarily observed during the input signal transition, $V_{tn}<V_{in}<V_{DD} + V_{tp}$ as illustrated in figure 2

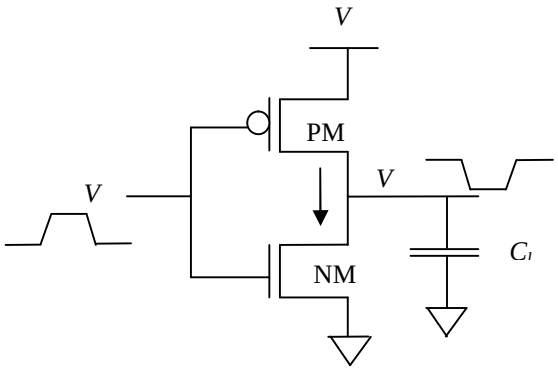



Fig. 2 Both NMOS and PMOS transistors may conduct a short–circuit current during Switching

Short-circuit current is a function of the output load and the rise and fall times of the input and output signals. The short-circuit current can be significant when the rise and fall times of the input signals are significantly larger than the output rise and fall times as the short - circuit current path will exist for a longer period of time.

The time-averaged short circuit current drawn from the power supply is given by:

$$I_{avg}\,(short\text{-}circuit) = \frac{1}{12}\frac{k.\tau.f_{clk}}{V_{DD}}(V_{DD}-2V_T)^3$$

Where $\tau$ = input rise and fall time.

The short-circuit power typically contributes to less than 10% of the total power consumed in a CMOS circuit provided that the input slew rate is higher than the output slew rate. The short-circuit power consumption can dominate the total power consumption of a CMOS circuit if the output is lightly loaded. Similarly, the short-circuit power consumption can be as high as the dynamic switching power consumption if the input signal rise and fall times are unusually long.

In addition to the three major sources of power consumption in CMOS digital integrated circuits, some chips may also contain components or circuits which actually consume static power. One example is the pseudo-nmos logic circuit. The presence of such circuit blocks should also be taken in to account when estimating the overall power dissipation of a complex system.

## III. Low Power VLSI Design Methodologies

In order to optimize the power dissipation of digital systems, low- power methodology should be applied throughout the design process from system level to process level, while realizing that performance is still essential.

- Power Reduction Through Process Technology
- Power Reduction through Circuit/Logic Design
- Power Reduction through Architectural Design
- Power Reduction through Algorithm Selection
- Power Reduction in System Integration

## IV. Power Reduction through Circuit/Logic Design

Among the various approaches for low-power VLSI design, we have focused on the power through circuit/logic design approach. We used clocked logic for low power applications called "Clocked Transmission Gate Adiabatic logic (CTGAL**)"** to achieve lower power consumption**.**

*A. Origin of ADIABATIC Logic:*

The word *ADIABATIC* comes from a Greek word that is used to describe thermodynamic processes that exchange no energy with the environment and therefore, no energy loss in the form of dissipated heat.

*B. Principle of ADIABATIC Switching:*

The word *ADIABATIC* comes from a Greek word that is used to describe thermodynamic processes that exchange no

energy with the environment and therefore, no energy loss in the form of dissipated heat. In real-life computing, such ideal process cannot be achieved because of the presence of dissipative elements like resistances in a circuit. However, one can achieve very low energy dissipation by slowing down the speed of operation and only switching transistors under certain conditions. The signal energies stored in the circuit capacitances are recycled instead, of being dissipated as heat. The adiabatic logic is also known as *ENERGY RECOVERY CMOS*. With the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can sometimes be used to reduce the power dissipation of the digital systems.

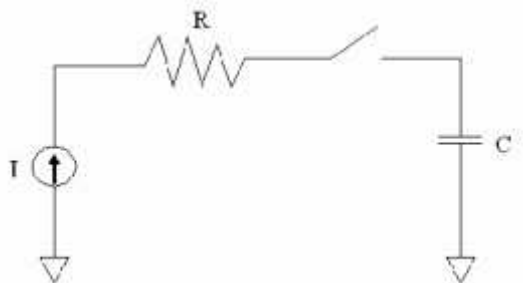



Fig. 3 Circuit explaining Adiabatic Switching

Here, the load capacitance is charged by a constant-current source instead of the constant voltage source as in the conventional CMOS circuits.

Here, $R$ is the resistance of the PMOS network. A constant charging current corresponds to a linear voltage ramp.

Assume, the capacitor voltage $V_C$ is zero initially

$\therefore$The voltage across the switch = $IR$

$P(t)$ in the switch = $I^2R$

$\therefore$Energy during charge = $(I^2R)T$

$$Also, \because I = \frac{CV}{T} \Rightarrow T = \frac{CV}{I}$$

$$E = \left(I^2R\right)T = \left(\frac{CV}{T}\right)^2 RT = \frac{C^2V^2R}{T}$$

$$Hence, E = Ediss = \left(\frac{CT}{T}\right)^2 RT$$

Where, the various terms of Equation are described as follows:

$E$ — energy dissipated during charging,

$Q$ — charge being transferred to the load,

$C$ — value of the load capacitance,

$R$ — resistance of the MOS switch turned on,

$V$ — final value of the voltage at the load,

$T$ — time spent for charging.

Now, a number of observations can be made as follows:

The dissipated energy is smaller than for the conventional case, if the charging time $T$ is larger than $2RC$. That is, the dissipated energy can be made arbitrarily small by increasing the charging time, the dissipated energy is proportional to $R$, as opposed to the conventional case, where the dissipation depends on the capacitance and the voltage swing. Thus, reducing the on-resistance of the PMOS network will reduce the energy dissipation.

*C. A Simple ADIBATIC Logic Gate:*

To convert a conventional CMOS logic gate into an adiabatic gate, the pull-up and the pull-down networks must be replaced with complementary transmission-gate (T-gate) networks. The T-gate network implementing the pull-up function is used to drive the true output of the adiabatic gate, while the T-gate network implementing the pull-down function drives the complementary output node. Note that all the inputs should also be available in complementary form. Both the networks in the adiabatic logic circuit are used to charge-up as well as charge-down the output capacitance, which ensures that the energy stored at the output node can be retrieved by the power supply, at the end of each cycle. To allow adiabatic operation, the DC voltage source of the original circuit must be replaced by a pulsed-power supply with the ramped voltage output.

*D. Power supply for an ADIABATIC logic gate:*

Instead of using a DC power supply, adiabatic CMOS circuits are driven by Alternating Current (AC) power supplies. In this way, the resonant tank is formed by the inductor in the power clock generator and the node capacitances in the adiabatic circuit to make energy transmission become magnetic energy → electric energy → magnetic energy, so the charge of the node capacitances can be recycled to achieve power recovery, and the irreversible energy conversion from electric energy to heat caused by dissipative elements, *i.e*. resistances, can be largely reduced or avoided.

*1) Design of Two Phases Sinusoidal Power Clock:* Power clocks not only supply energy for adiabatic circuits, but also control the work rhythm of adiabatic circuits, so it is demanded that the phases of power clocks be stable, and the phase error not be very large; otherwise evaluation and energy recovery of the output loads cannot perform completely, and it results in the relatively large non-adiabatic energy consumption. Therefore it is obvious that a power clock generator is such an important part of an adiabatic circuit.

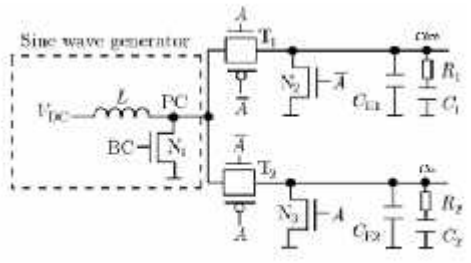



Fig.4 Two-phase sinusoidal power clock generator

## V. DESIGN AND WORKING OF CLOAKED TRANSMISSION GATE ADIABATIC LOGIC (CTGAL)

For CTGAL circuits, the two-phase sinusoidal power clocks *Clk* and *Clkb* are generated by the circuit and their phase difference is $180^0$.

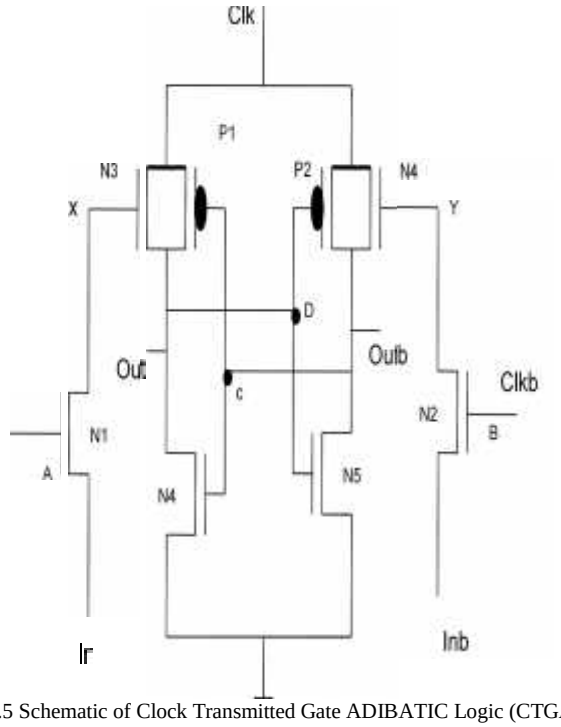



Fig.5 Schematic of Clock Transmitted Gate ADIBATIC Logic (CTGAL)

one period of the power clock is divided into four equal parts $T_1$, $T_2$, $T_3$, and $T_4$.During the period $T_1$, the voltages of the input signal *In* and the clock-controlled clock *Clkb* go high, but the voltages of the input signal *In* and the power clock *Clk* are low. Therefore, $N_1$ is turned on (it operates in the saturation region), and the voltage of the node *x* is charged to about $V_{DD}-V_{TN}$ where $V_{TN}$ is the threshold voltage of the NMOS transistor. At the same time, $N_2$ is turned on so as to make the voltage of the node *y* 0V. As the voltage of the power clock *Clk* is 0V, the voltages of the outputs keep at 0V. During this period, the input signals are sampled by the clock-controlled clock *Clkb*. During the period $T_2$, the voltage of *Clkb* descends so that $N_1$ is turned off and the voltage of the node *x* is still at $V_{DD}-V_{TN}$. Therefore, the period $T_1$-$T_2$ can be generally termed the sampling period when the input signals are sampled.

During the period $T_3$ (the logic evaluation period), the voltage of *Clkb* is 0V, but the voltage of the power clock *Clk* begins to go high. $N_1$ and $N_2$ are turned off so as to make the nodes *x* and *y* keep a floating state where *x* is the floating high-voltage node and *y* is the floating low-voltage node, and consequently $N_3$ is turned on, so the output node *Out* follows the power clock *Clk* to rise. When the voltage of *Out* rises above $V_{TN}$, $N_6$ is turned on and *Outb* is clamped to the ground (0V).

When the voltage of the power clock *Clk* rises above $|V_{TP}|$, where $V_{TP}$ is the threshold voltage of the PMOS transistor, $P_1$ is turned on, so *Clk* charges *Out* through the complementary transmission gate composed of $N_3$ and $P_1$ in a fully adiabatic manner.

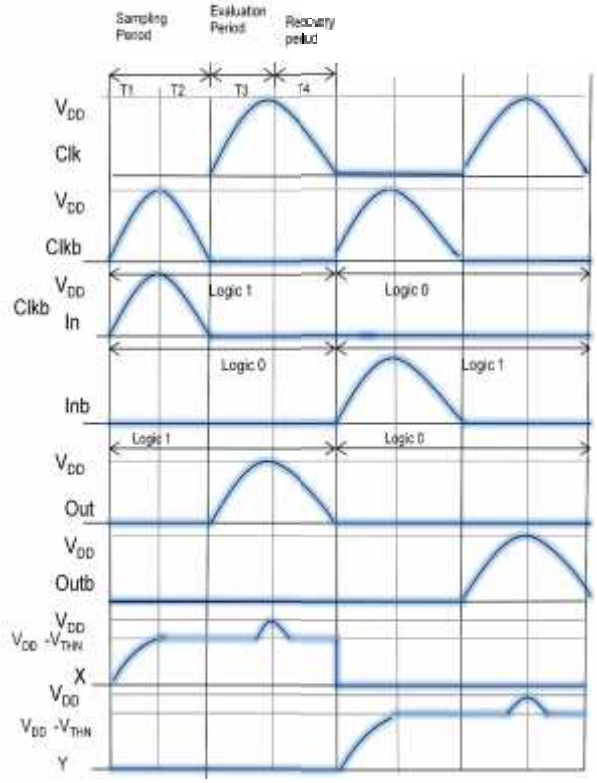



Fig.6 Waveform of CTGAL

During the period $T_4$ (the energy recovery period),*Out* follows *Clk* to drop to 0V through the complementary transmission gate composed of $N_3$ and $P_1$, and the charge on the node *Out* is recovered to the power clock *Clk* in a fully adiabatic manner. During the period $T_3$-$T_4$, the voltages of the input signals and the clock-controlled signals are 0V, therefore $N_1$ and $N_2$ are turned off, and the nodes *x* and *y* keep a floating state. When the voltage of *Clk* descends from $V_{DD}$ to 0V, the voltage of the node *x* descends by $\Delta V$, namely, the voltage of *x* comes back to $V_{DD}-V_{TN}$ finally. So during the energy recovery period, when $P_1$ is turned off, $N_3$ is still turned on so as to ensure that the charge on the output node *out* can be recovered to *Clk* completely.

## VI. DESIGN AND SIMULATION OF INVERTER USING CMOS AND CTGAL LOGIC

### *A. CMOS based inverter:*

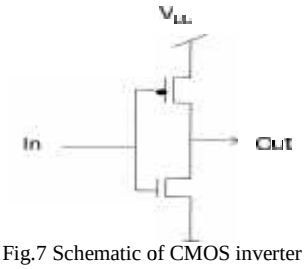



Fig.7 Schematic of CMOS inverter

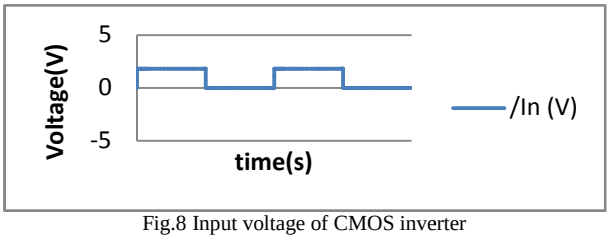



Fig.8 Input voltage of CMOS inverter

The input for the CMOS is a square wave which varies from 0 to near 1.75 volt.

The output of the inverter is given by the following graph

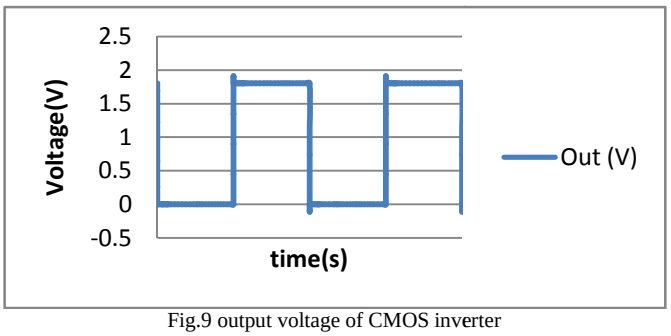



Fig.9 output voltage of CMOS inverter

*B. CTGAL based inverter:*

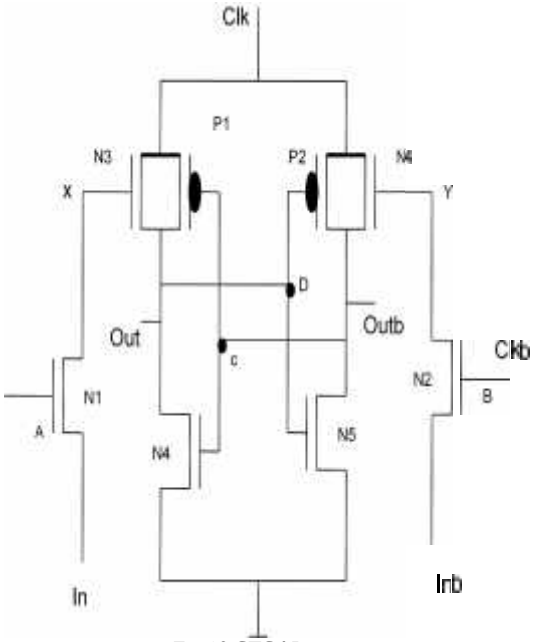



Fig.10 CTGAL inverter

Output and input waveform for the CTGAL is given by following graphs

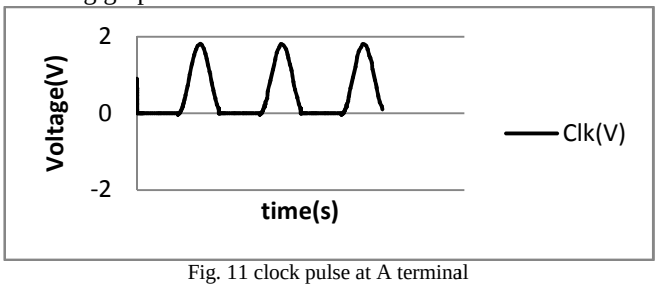



Fig. 11 clock pulse at A terminal

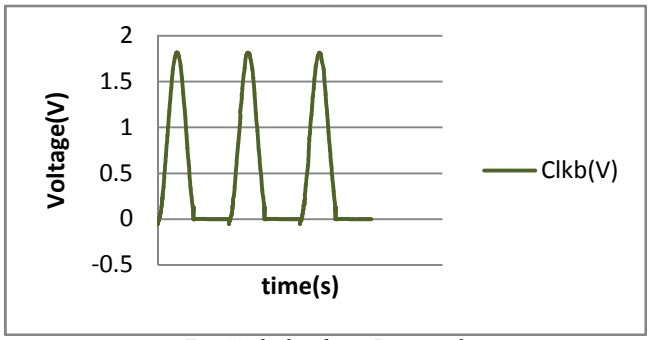
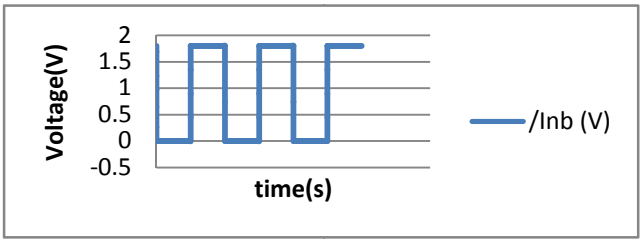



Fig. 12 clock pulse at B terminal

Fig. 13 output of CTGAL based inverter




## VII. DESIGN OF 4-BIT CARRY LOOK ADDER

The 4-bit Carry Look Adder (CLA) based on conventional CMOS and Clocked Transmission Gate Adiabatic logic (CTGAL) is designed in Cadence Virtuoso analog design environment using 0.18um CMOS Technology with the supply voltage of 1.8 V.

*A. Design of 4-BIT CARRY LOOK ADDER using CMOS:*

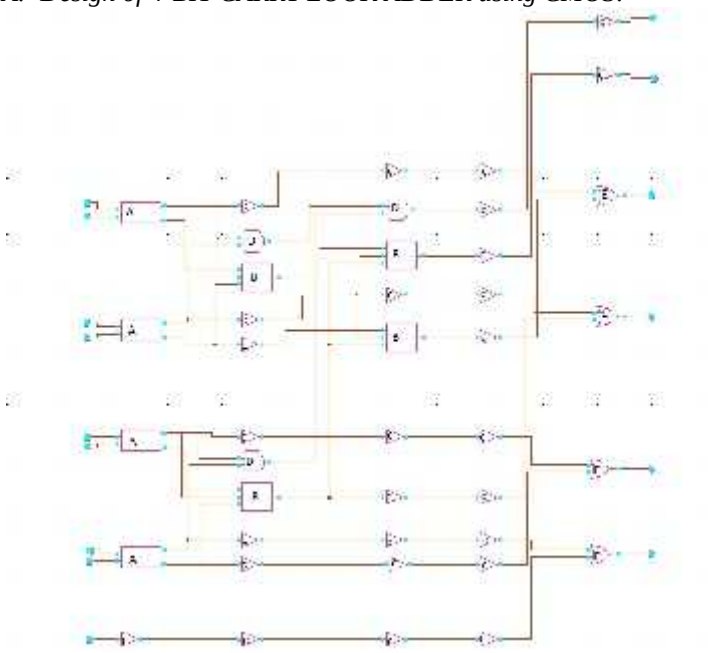


Fig. 14 Schematic of 4-bit Carry look Adder Based on CMOS

In the Above schematic block A represents (A XOR B) and (A AND B) operation. Block B represents logic A+BC, block C represents buffer, block D represents 2-input AND gate and block E represents two input XOR gate.

*B. Design of 4-BIT CARRY LOOK ADDER using CTGAL:*

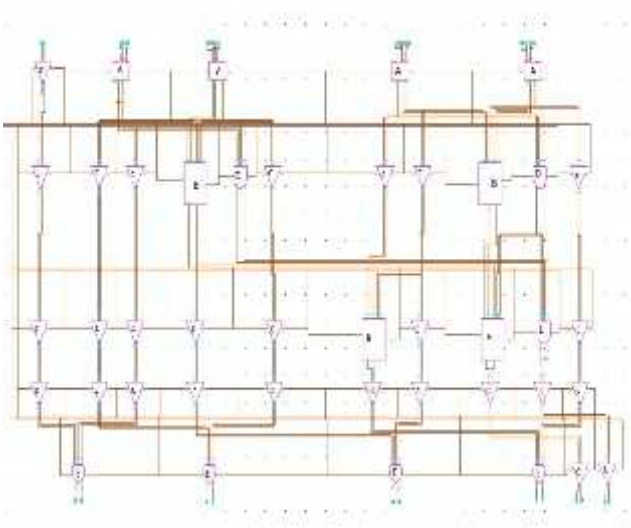


Fig. 15 Schematic of 4-bit Carry look Adder Based on CTGAL

In the Above Fig. 15 block A represents (A XOR B) and (A AND B) operation. Block B represent logic A+BC based on CTGAL, block C represents Schematic of Inverter based on CTGAL, block D represents Schematic of Two-input AND Gate based on CTGA and block E represents Schematic of a Two-Input CTGAL based XOR Gate.

*1). Comparison of power dissipation between CMOS and CTGAL based 4-BIT LOOK ADDER with different frequency:* This section deals with the comparison of power dissipation and for 4-bit Carry Look Adder based on the full complementary CMOS logic style and the ultra low-power Clocked Transmission Gate adiabatic logic style with different frequency.

| **Frequency(MHz)** | **Power Dissipation** | |
|---|---|---|
| | CTGAL | CMOS |
| **10** | 1.52E-05 | 2.94E-03 |
| **20** | 2.38E-05 | 3.51E-03 |
| **50** | 6.87E-05 | 5.23E-03 |
| **100** | 9.58E-05 | 8.08E-03 |

Fig.16 Dynamic Power dissipated by Static CMOS and Adiabatic CTGAL for 4-bit look adder

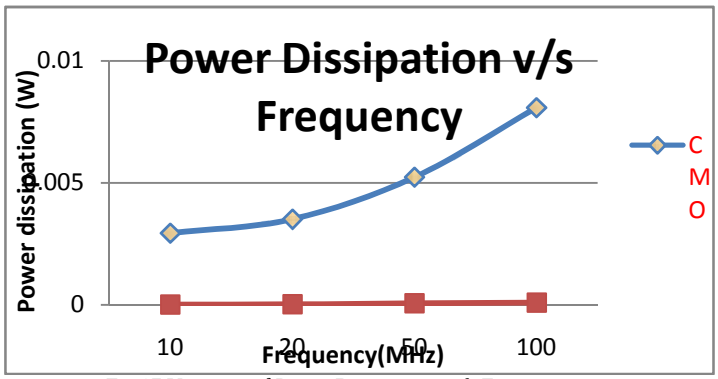



Fig.17 Variation of Power Dissipation with Frequency

We can seen from the above fig. 17 that power dissipation is increase in CMOS based circuit with increase in frequency but in CTGAL based circuit it is zero

*2). Delay with Frequency:* This section deals with the comparison of delay for 4-bit Carry Look Adder based on the full complementary CMOS logic style and the ultra low-power Clocked Transmission Gate adiabatic logic style with different frequency.

| **Frequency(MHz)** | **Delay (Nanosecond )** | |
|---|---|---|
| | CTGAL | CMOS |
| **10** | 150 | 3.23 |
| **20** | 75 | 3.1 |
| **50** | 30 | 3.1 |
| **100** | 15 | 2.9 |

Fig.20 Delay caused by Static CMOS and Adiabatic CTGAL for 4-bit CLA

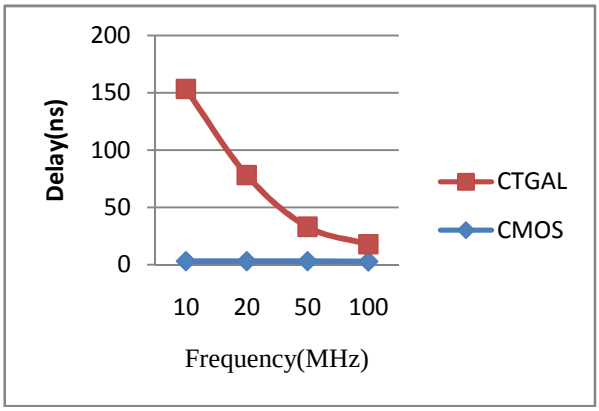



Fig.19 Variation of Delay with Frequency

## VIII. RESULT

As the simulation result for 4-Bit CARRY LOOK ADDER the power dissipation is greatly reduced by using ADIABATIC logic.

## IX. CONCLUSION

The thesis primarily was focused on the design of low power CMOS cell structures, which is the main contribution of this work. The design of low power CMOS cell structures uses fully complementary CMOS logic style and an adiabatic CTGAL logic style. The basic principle behind implementing various design units in the two logic styles is to compare them with reference to the average power dissipated by all of them.

A family of full-custom conventional CMOS Logic and Adiabatic Logic units was designed in IC design environment provided by Cadence using TSMC 0.18 um technology and the analysis of the average dynamic power dissipation with respect to the frequency done. It was found that the adiabatic CTGAL logic style is advantageous in applications where power reduction is of prime importance as in high performance battery-portable digital systems running on batteries such as note-book computers, cellular phones and personal digital assistants.

With the CTGAL approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can be used to reduce the power dissipation of the digital systems. With the help of CTGAL, the energy savings of up to 80 -90 % in case of four bit carry look adder and up to 50-55% in case of eight bits Barrel shifter can be reached.

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