FPGA based generalized architecture for Modulation and Demodulation Techniques

Swapan K Samaddar[#1], Atri Sanyal[#2], Somali Sanyal[#3]

#1Genpact India, Kolkata, West Bengal, India, swapansamaddar@gmail.com
#2NSHM College of Management & Technology, Kolkata, West Bengal, India, atri.sanyal@nshm.com
#3B.P. Poddar College of Engineering & Management, Kolkata, West Bengal, India, s somali@rediffmail.com

***Abstract*- Here we design a modulator-demodulator circuit which can execute different modulation schemes like- AM, ASK, BPSK, FSK & QPSK. Both the LUT based implementation and complete VHDL based implementation have done by using digital high frequency carriers. In the first step to realize the whole modulation and demodulation schemes using MATLAB Simulink. The format of a VHDL program is built around the concept of BLOCKS which are the basic building units of a VHDL design.**

Key words: AM, ASK, BPSK, FSK, QPSK, VHDL, LUT

1. INTRODUCTION

The objective of this paper is to design a modulator-demodulator circuit which can execute different modulation schemes like- AM, ASK, BPSK, FSK & QPSK. According to many literature surveys it can be seen that the work done so far was mainly based on storing the sampled digital value of analog carrier to implement any modulation technique. For example a paper by **Michal Kováč** [1] to implement the modulator in the FPGA used VHDL language and DDS (Direct Digital Synthesizer) component in the Xilinx ISE development tool. But in this paper both the LUT based implementation and complete VHDL based implementation have done by using digital high frequency carriers. In the first step to realize the whole modulation and demodulation schemes using MATLAB Simulink. The modulation schemes are AM, ASK, BPSK, FSK & QPSK. In the next step to design AM & QPSK using VHDL. This hardware description is used to configure a programmable logic device (PLD), such as a field programmable gate array (FPGA), with a custom logic design. The general format of a VHDL program is built around the concept of BLOCKS which are the basic building units of a VHDL design. Within these design blocks a logic circuit of function can be easily described.

2. THE MODULATOR AND DEMODULATOR ARCHITECTURE

AM:- Amplitude modulation is defined as the process in which amplitude of the carrier wave is varied about a mean value, linearly with the base band signal. Amplitude modulation is a linear modulation.

Note that the AM signal is of the form

$A(1+\beta \sin \omega_m t) \cos(\omega_c t)$

$= A \cos \omega_c t + AB/2(\cos((\omega_c + \omega_m)t) + \cos((\omega_c - \omega_m)t))$

This has frequency components at frequencies ω_c, $\omega_c + \omega_m$, $\omega_c - \omega_m$.

ASK: ASK describes the technique where the carrier wave is multiplied by the digital signal *f(t)*. Mathematically, the modulated carrier signal is *s(t)*:

$S(t) = f(t) \sin(2\pi f_c t + \varphi)$

BPSK: In BPSK modulation the carrier phase acquires two discrete states (0° and 180°), which correspond to one bit of the modulation signal. Therefore the symbol period is equal to the bit period $T_s = T_b$. The BPSK modulated output is expressed as:

$s(t) = \square\, m(t).\cos(2\pi f_c t \square + \varphi \square)$,

where $m(t)$ is a modulation base band signal ±1, f_c is a carrier frequency and $\square$ is aninitial phase.

FSK: In FSK system, two sinusoidal carrier waves of the same amplitude Ac but different frequencies fc1 and fc2 are used to represent binary symbols 1 and 0 respectively.

$S(t) = Ac \cos(2\pi f_{c1} t)$ symbol 1

$= Ac \cos(2\pi f_{c2} t)$ symbol 0

QPSK**:** In QPSK modulation the carrier phase acquires four discrete states (±45° and ±135°), which correspond to a couple of modulation signal bits. The symbol period is twice the bit period $T_s = 2.T_b$. QPSK is an extension of binary PSK. In binary data transmission, we transmit only one of two possible signals during each bit interval T_b .On the other hand, in an M-ary data transmission it is possible to send any one of M possible signals, during each signaling interval T.

In most of cases, the no of possible signal is:

$M=2^n$

Where n is an integer.

The signaling interval is

$T=nT_b$

3. DESIGN METHODOLOGIES

The design of a system is essentially the blueprint or a plan for a solution for the system. Here in the first step I have designed the whole system using MATLAB Simulink. A Matlab-Simulink simulation model is described that enables an accurate performance prediction of complete modulations and demodulations schemes. In the next step to built the basic units in FPGA using HDL coding.

The whole problem is broken down to smaller sub modules as below-

i> Identifying the Basic Building Blocks (BBB) of various communication schemes.

ii> Design the BBB using Matlab Simulink with proper specifications.

iii> Developing an efficient routing mechanism using MUX.

iv> Converting different analog Circuits to its digital equivalent circuits.

v> Getting digital equivalent output of an analog signal by sampling quantizing and coding using ‘C’ program.

vi> Designing all the basic units in FPGA using VHDL coding.

However the different pieces cannot be entirely independent of each other, as they together form the system. The different pieces have to cooperate and communicate to solve the larger problem.

The Modulator:- The modulator which is designed here is a analog modulator which basically uses analog components. Here in the first step I have considered all the basic components of all the modulation schemes and I have taken all the similar & different parts of the various modulation schemes and considered them as Basic Building Blocks (B.B.B.). With this B.B.B. and some router or switches I have built a model so that according to the requirement we can get different modulation schemes. So for this we have considered some control signals and varying these signals we can get different modulation schemes.

Basic building blocks:-

Different Low Pass Filter(Different Cut Off Frequencies), High Pass Filter , Inverter, Integrator, Adder, Multiplier., Pulse Wave Generator, Sine Wave Generator:- Local Oscillator, Band Pass Filter, Unipolar To Bipolar Converter, Multi Port Switches With Different Control Signals :, Butterworth Filter (LPF.) Order 2, Transfer Function =1/(S+1), Phase shifter, Comparator, Message signal:- different wave generator, Control switches.

Here the model of control switches is as follow:- Basic components :- de multiplexer ,

Scheme	Control signals										
	C0C1	C2	C3	C4	C5	C6C7	C8C9	C11	C12	C13C14	C15
A.M	00/10	1	0	1	1	11	001	0	--	--	00
ASK	01	1	1	1	1	11	100	0	--	--	00
BPSK	01	1	1	1	0	11	011	0	--	--	00
FSK	01	0	1	1	1	00	000	0	01	00	01
QPSK	01	1	1	1	1	10	011	0	01	10	01

MOSFET

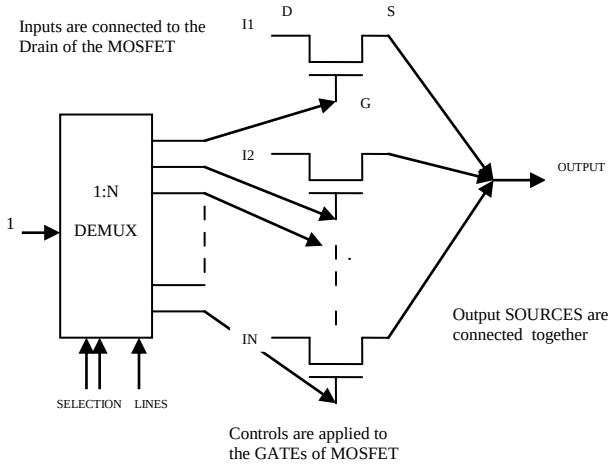

Fig 1: Control Switch

Table 1: The control logic in Modulator

Scheme	Control signals												
	M0M1M2	M3M4M5	M6M7M8	M9	M10	M11	M12	M13M14	M15	M16M17	M18		
A.M	000	000	------	0	1	--	--	01	--	00	0		
ASK	001	001	------	0	1	--	--	01	--	00	1		
BPSK	010	010	------	0	1	--	--	01	--	00	1		
FSK	011	011	011	0	1	1	0	01	0	01	1		
QPSK	100	100	100	0	1	1	1	10	1	00	1		

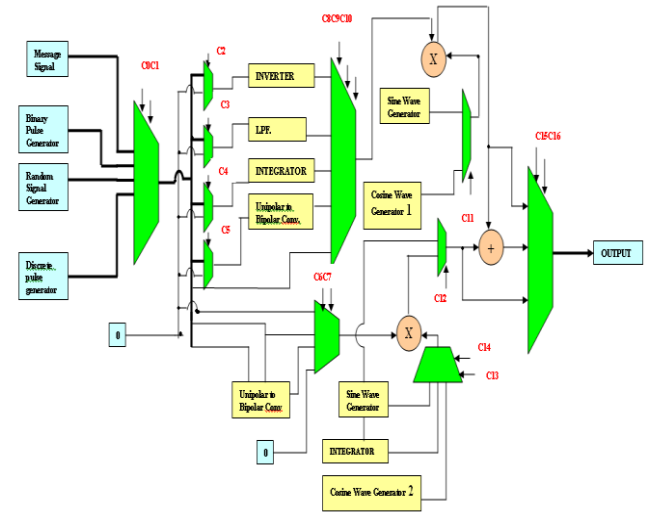

Fig 2: The MODULATOR (Designed in Matlab Simulink with analog components)

Table 2: The control logic in Demodulator

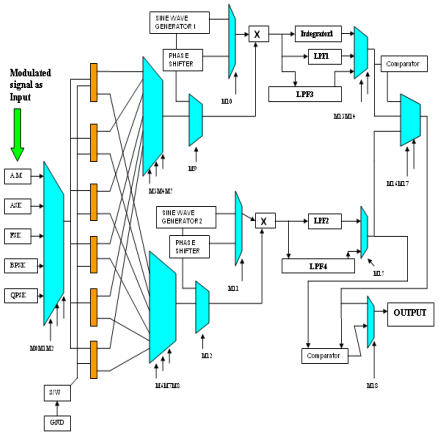

Fig3: The Demodulator (Designed in Matlab Simulink with analog components)

4. RESULT & ANALYSIS:

A. Utilization Factor Calculation:

i> Analog Modulation:-

Schemes	Number of operational amplifier	Utilization factor(%)
AM	6	28
ASK	5	23
BPSK	7	32
FSK	10	46

QPSK	12	55

Table3: Utilization Factor (Analog Modulation)

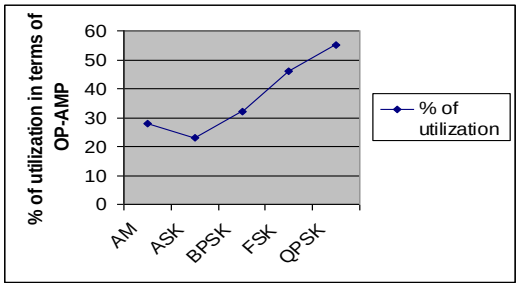

Fig 4: Utilization Factor (Modulation)

ii> Analog De-Modulation:-

Schemes	Number of operational amplifier	Utilization factor(%)
AM	5	30
ASK	6	36
BPSK	6	36
FSK	11	65
QPSK	14	83

Table4: Utilization Factor (Demodulation)

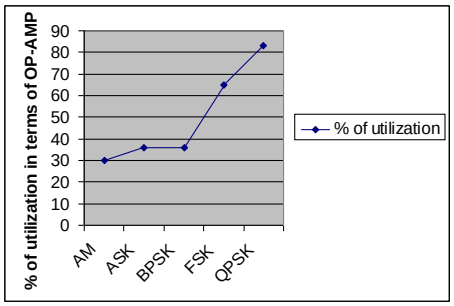

Fig 5: Utilization Factor (Demodulation)

B. FPGA Results:- on different schemas

Schemes	Number of Slices	Number of Slice of Flip flop	Number of 4 input LUTS	Number of Bonded IOBs:
AM	28	45	49	38
ASK	2	4	1	8
BPSK	3	5	1	10
FSK	3	5	1	10
QPSK	7	12	2	13

Comparis

Table 5: Comparison among Device utilization

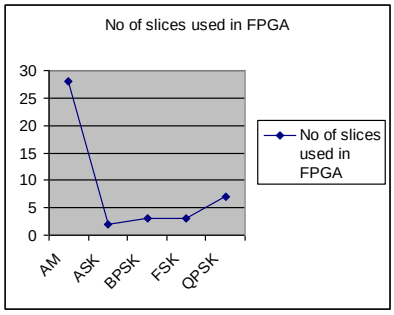

Fig 6: Comparisons among Different Schemes (in terms of Slices)

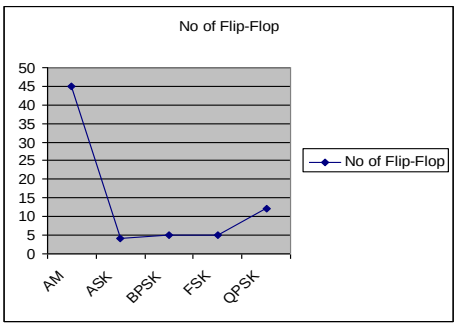

Fig 7: Comparisons among Different Schemes (in terms of Flip-Flop)

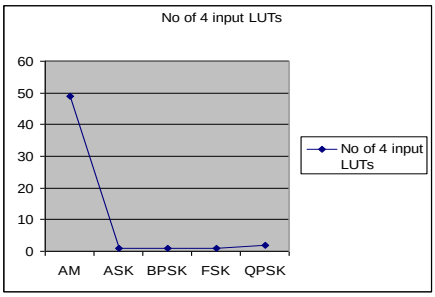

Fig 8: Comparisons among Different Schemes (in terms of 4 input LUTS)

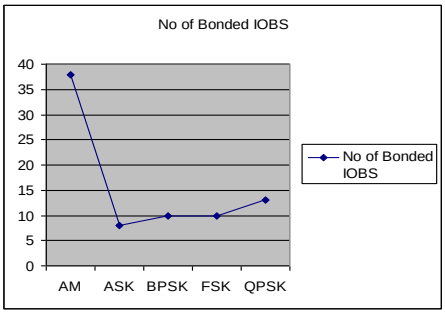

Fig 9: Comparisons among Different Schemes (in terms of No. of bonded IOBs)

Basic Unit	No. of operational Amplifier	Other components
Comparator	1	Resistances
Unipolar To Bipolar Converter	2 (1 For Clamper & 1 For Gain)	Resistances , Capacitance, Diode
Adder	1	Resistances
Integrator	1	Resistances , Capacitance
Lpf1	1	Resistances , Capacitance
Lpf2	1	Resistances , Capacitance
Butterworth LPF Of Order 2	1	Resistances , Capacitance
Square Wave Generator	1	Resistances, Capacitance, Diodes.
Sine Wave Generator	1	Resistances , Capacitances, Diode, JFET
Multiplier	3	
Inverter		MOSFET

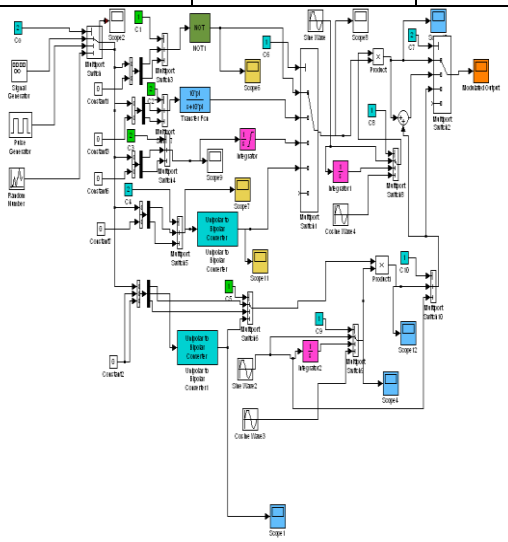

Fig 10: Modulator

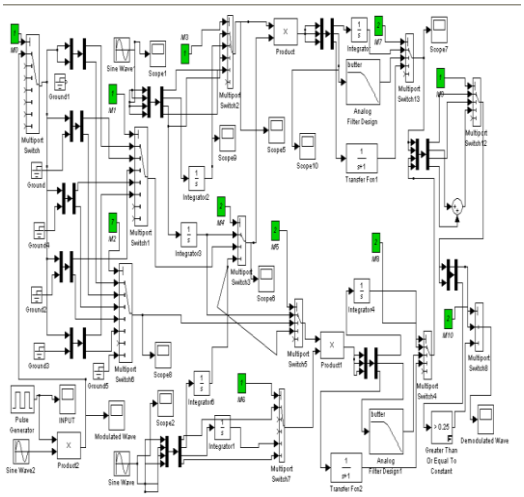

Fig11: Demodulator

C. *CALCULATION OF UTILIZATION FACTOR IN TERMS OF OPERATIONAL AMPLIFIER*

Table 7:No of Operational Amplifiers required for basic units

Therefore number of operational amplifier in modulator circuit:-22

Schemes	Number of operational amplifier	Utilization factor (%)
AM	6	28
ASK	5	23
BPSK	7	32
FSK	10	46
QPSK	12	55

Table 8: Comparison of different schemes of modulator circuits.

Therefore number of operational amplifier in demodulator circuit:-17

Schemes	Number of operational amplifier	Utilization factor (%)
AM	5	30
ASK	6	36
BPSK	11	65
FSK	6	36
QPSK	14	83

Table 9: Comparison of different schemes of demodulator circuits.

5. CONCLUSION & FUTURE WORK

1. In this project a modulator and demodulator circuit of various modulation schemes and FPGA realization of AM, ASK, BPSK, FSK, QPSK on FPGA has been implemented.
2. The modulator and demodulator have been designed will give different schemes and one only need to change the control signals to get a specific modulation technique.
3. The FPGA realization has been implemented is based on total digital techniques and the realization needs only digital circuits. The carrier used is also digital high frequency square wave signal. As a result the total realization is much faster than other technique which uses Analog signals and Analog circuits.
4. In future it is possible to develop a complete FPGA based modulation and demodulation technique what I have realized completely in MATLAB Simulink and partially in FPGA.

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